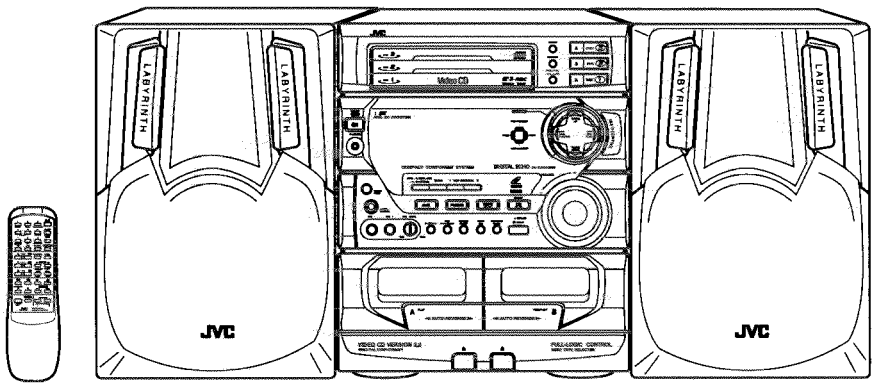
JVC

# SERVICE MANUAL

## COMPACT COMPONENT SYSTEM

# MX-V508T/MX-V588T

| Area Suffix | |
|---|---|
| U | Other Areas |
| US | Singapore |
| UT | Taiwan |
| UB | Hong Kong |
| UF | China |



COMPACT disc DIGITAL AUDIO

COMPACT disc DIGITAL AUDIO GRAPHICS

COMPACT disc DIGITAL VIDEO

PlayBack Control

## Contents



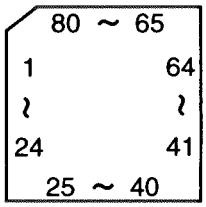


No.20714
Aug. 1998

# Description of Major ICs

## ■UPD78044FGF-089(IC701):System Control Micon

1.Trminal Layout




2.Pin Function

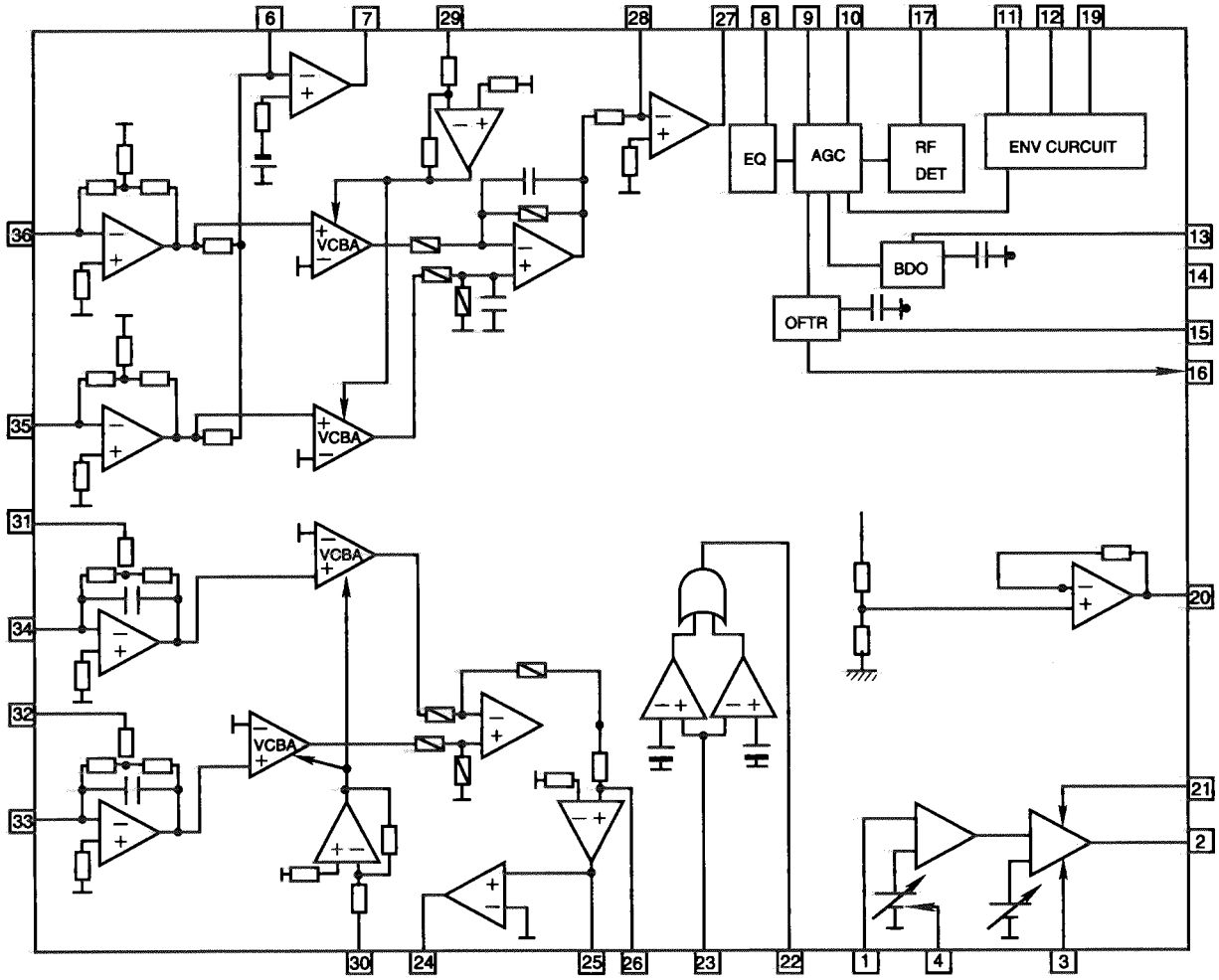
| Pin No. | Symbol | I/O | Function | Pin No. | Symbol | I/O | Function |
|---|---|---|---|---|---|---|---|
| 1~7 | 7G~1G | O | FL Grid control signal | 39 | $\overline{+BCTL}$ | O | 5V switch |
| 8 | VDD | - | Power supply +5V | 40 | MRESET | O | Reset signal output. |
| 9 | SCKO | O | Serial Clock (PLL.SLC.Vol.C3) | 41 | OSCK | O | Clock signal to IC106 |
| 10 | SDATAO | O | Serial data (PLL.SLC.Vol.C3) | 42 | OSCS | O | Chip select signal to IC106 |
| 11 | $\overline{FAUX}$ | O | AUX Indicator control | 43 | OSD | O | Micon command data to IC251 |
| 12 | $\overline{LED\ TAPE}$ | O | TAPE Indicator control | 44 | DSPSTB | O | Strobe changer control |
| 13 | SLC-STTA | O | Strobe Tape control | 45 | OSDATA | O | OS Data to IC106 |
| 14 | MCLK | O | Sub code clock | | | | |
| 15 | MCMND | O | CD Mecha command data | 46 | POUT | O | Power on/off |
| 16 | MSTAT | I | Sub code data | 47 | REM | I | Remote control |
| 17 | $\overline{REST}$ | I | System reset signal | 48 | ICVss | - | To ground |
| 18 | PHOTO A | I | Tape A mechanism running detection | 49 | $\overline{SMUTE}$ | O | System mute |
| 19 | PHOTO B | I | Tape B mechanism running detection | 50 | MRDY | O | Ready signal to IC251 |
| 20 | AVss | - | AD Ground | 51 | F.TU | O | Function TUNER |
| 21 | NC | I | TEST (Normally "H") | 52 | Vdd | - | Power supply +5V |
| 22 | SAFETY1 | I | Trouble detection | 53 | VOL- | I | Volume encorder input (-) |
| 23 | SLC KEY3 | I | Tape A playback detect switch | 54 | VOL+ | I | Volume encorder input (+) |
| 24 | SLC KEY2 | I | Tape B playback detect switch | 55 | SPK | O | Speaker relay control signal |
| 25 | SLC KEY1 | I | Tape B playback/REC detect switch | 56 | PROTECTOR | I | Protector input |
| 26~28 | KEY3~1 | I | Key matrix input | 57 | BACKUP | I | Backup detect |
| 29 | AVdd | - | AD+5V | 58 | LATCH | O | Latch signal to IC302 |
| 30 | AVREF | - | AD REF + 5V | 59 | PERIOD | O | Tuner PLL strobe |
| 31 | XT1 | I | Sub clock 32.768kHz | 60~70 | S1~S11 | O | FL segment control signal |
| 32 | XT2 | O | Sub clock 32.768kHz | 71 | VLOAD | - | Supply voltage for FL drive |
| 33 | Vss | - | To ground | 72~76 | S12~S16 | O | FL segment control signal |
| 34 | X1 | I | Main clock 4.19MHz | 77~79 | 11G1~9G1 | O | FL grid control signal |
| 35 | X2 | O | Main clock 4.19MHz | 80 | 8G | O | FL grid control signal |
| 36 | BEAT | O | Main clock shift | | | | |
| 37 | MSI | I | Music scan | | | | |
| 38 | $\overline{MPX}$ | I | Stereo detect | | | | |

## ■ AN8806SB(IC601):RF&Servo AMP

1.Treminal Layout

| | | | |
|---|---|---|---|
| PD | 1 | 36 | PDAC |
| LD | 2 | 35 | PDBD |
| LDON | 3 | 34 | PDF |
| LDP | 4 | 33 | PDE |
| VCC | 5 | 32 | PDER |
| RF- | 6 | 31 | PDFR |
| RF OUT | 7 | 30 | TBAL |
| RF IN | 8 | 29 | FBAL |
| C.AGC | 9 | 28 | EF- |
| ARF | 10 | 27 | EF OUT |
| C.ENV | 11 | 26 | TE- |
| C.EA | 12 | 25 | TE OUT |
| CS BDO | 13 | 24 | CROSS |
| BDO | 14 | 23 | TE BPF |
| CS BRT | 15 | 22 | VDET |
| OFTR | 16 | 21 | LD OFF |
| /NRFDET | 17 | 20 | VREF |
| GND | 18 | 19 | ENV |

2.Block Diagram

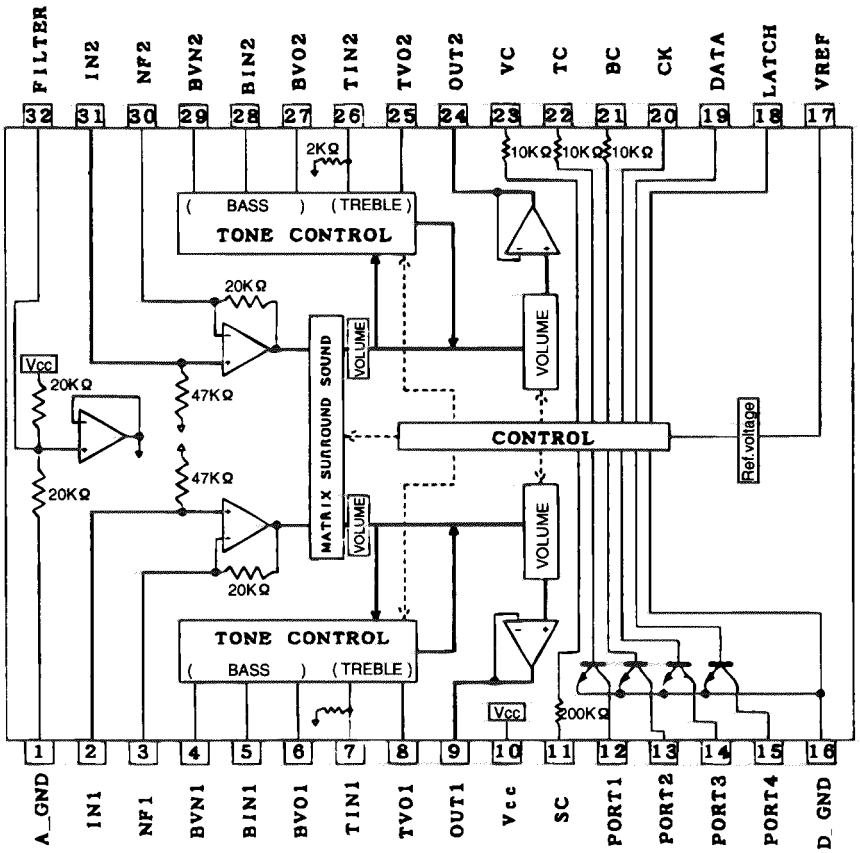


3. Functions

| Pin No. | Symbol | I/O | Functions and operations |
|---|---|---|---|
| 1 | PD | I | APC amp input terminal |
| 2 | LD | O | APC amp output terminal |
| 3 | LD ON | I | APC ON/OFF control terminal |
| 4 | LDP | -- | Connect to ground |
| 5 | VCC | -- | Power supply |
| 6 | RF- | I | Inverse input pin for RF amp |
| 7 | RF OUT | O | RFamp output |
| 8 | RF IN | I | RF input |
| 9 | C.AGC | I/O | Connecting pin of AGC loop filter |
| 10 | ARF | O | RF output |
| 11 | C.ENV | I/O | A capacitor is connected to this terminal to detect the envelope of RF signal |
| 12 | C.EA | I/O | A capacitor is connected to this terminal to detect the envelope of RF signal |
| 13 | CS BDO | I/O | A capacitor is connected to detect the lower envelope of RF signal |
| 14 | BDO | O | BDO output pin |
| 15 | CS BRT | I/O | A capacitor is connected to detect the lower envelope of RF signal |
| 16 | OFTR | O | Of-track status signal output |
| 17 | /NRFDET | O | RF detection signal output |
| 18 | GND | -- | Ground |
| 19 | ENV | O | Envelope output |
| 20 | VREF | O | Reference voltage output |
| 21 | LD OFF | -- | Connect to ground |
| 22 | VDET | O | Vibration detection signal output |
| 23 | TE BPF | I | Input pin of tracking error through BPF |
| 24 | CROSS | O | Tracking error cross output |
| 25 | TE OUT | O | Tracking error signal output |
| 26 | TE- | I | Inverse input pin for tracking error amp |
| 27 | FE OUT | O | Output pin of focus error |
| 28 | FE- | I | Inverse input pin for focus error amp |
| 29 | FBAL | I | Focus balance control |
| 30 | TBAL | I | Tracking balance control |
| 31 | PDFR | I/O | F I-V amp gain control |
| 32 | PDER | I/O | E I-V amp gain control |
| 33 | PDF | I | I-V amp input |
| 34 | PDE | I | I-V amp input |
| 35 | PD BD | I | I-V amp input |
| 36 | PD AC | I | I-V amp input |

## ■BH3854AS(IC302):VOLUME/EQUALIZER

1.Block Diagram

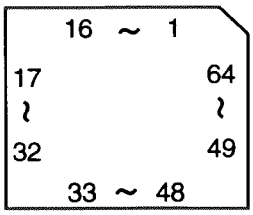



2.Pin Function

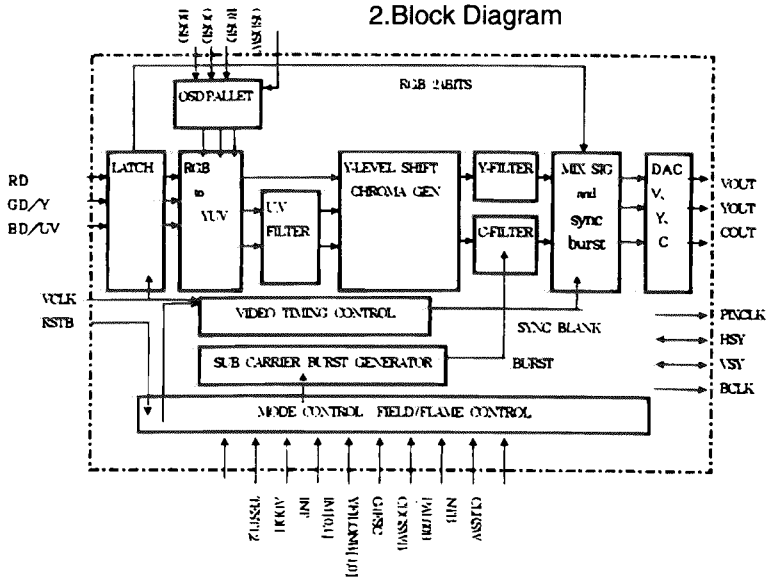
| Pin No. | Symbol | I/O | Function | Pin No. | Symbol | I/O | Function |
|---|---|---|---|---|---|---|---|
| 1 | A GND | - | Analog system ground. | 18 | LATCH | I | Receive latch data. |
| 2 | IN1 | I | 1ch volume input. | 19 | DATA | I | Termianl to receive data. |
| 3 | NF1 | - | Non connect | 20 | CLK | I | Terminal to receive clock. |
| 4 | BVN1 | - | 1ch Low-frequency filter. | 21~23 | BC,TC,VC | - | Time constant attachment for switching shock protection. |
| 5 | BIN1 | - | 1ch Low-frequency filter. | | | | |
| 6 | BVO1 | - | 1ch Low-frequency filter. | 24 | OUT2 | O | 2ch volume output. |
| 7 | TIN1 | - | 1ch High-frequency filter. | 25 | TVO2 | - | 2ch high-frequency filter. |
| 8 | TVO1 | - | 1ch High-frequency filter. | 26 | TIN2 | - | 2ch high-frequency filter. |
| 9 | OUT1 | O | 1ch volume output. | 27 | BVO2 | - | 2ch low-frequency filter. |
| 10 | VCC | - | Terminal for power supply. | 28 | BIN2 | - | 2ch low-frequency filter. |
| 11 | SC | - | Time constant attachment for switching shock protection. | 29 | BVN2 | - | 2ch low-freauency filter. |
| | | | | 30 | NF2 | - | Non connect. |
| 12~15 | PORT1~4 | O | Terminal for port output. | 31 | IN2 | O | 2ch volume output. |
| 16 | D GND | - | Digital system ground. | 32 | FILTER | I | Terminal for filter. |
| 17 | VREF | I | 3.8V reference voltage output. | | | | |

## ■BU1424K(IC104):Digital RGB Encoder

1.Terminal Layout




2.Block Diagram

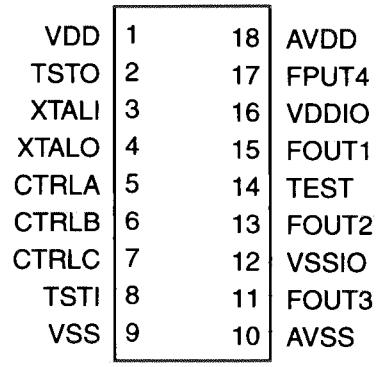



3.Pin Function

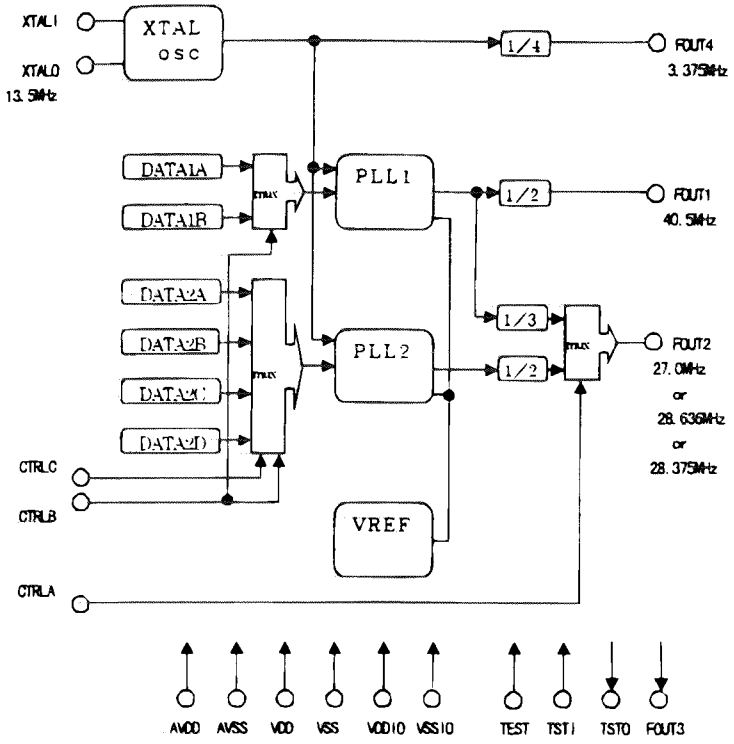
| Pin No. | Symbol | I/O | Function | Pin No. | Symbol | I/O | Function |
|---|---|---|---|---|---|---|---|
| 1 | BOSD | I | OSD blue data input. | 33 | SLABEB | | Select master/slave. |
| 2 | Y0 | I | Green data Bit0 (LSB). | 34 | ADDH | | +0.5/-0.5 line at Non-Inter. |
| 3 | Y1 | I | Green data Bit1. | 35 | VREF | - | DAC Bias. |
| 4 | Y2 | I | Green data Bit2. | 36 | CGND | - | Chroma output ground. |
| 5 | Y3 | I | Green data Bit3. | 37 | COUT | O | Chroma output. |
| 6 | Y4 | I | Green data Bit4. | 38 | VGND | - | Composite output ground. |
| 7 | Y5 | I | Green data Bit5. | 39 | VOUT | O | Composite output. |
| 8 | Y6 | I | Green data Bit6. | 40 | AVSS | - | Analog ground (DAC,VREF). |
| 9 | GND | - | Digital Ground. | 41 | AVDD | - | Analog (DAC) VDD. |
| 10 | Y7 | I | Green data Bit7 (MSB). | 42 | IR | I | Reference resistor. |
| 11 | C0 | I | Blue data Bit0 (LSB). | 43 | AVDD | - | Analog (VREF) VDD. |
| 12 | C1 | I | Blue data Bit1 (LSB). | 44 | YGND | - | Luminance output ground. |
| 13 | C2 | I | Blue data Bit2 (LSB). | 45 | YOUT | O | Luminance output. |
| 14 | C3 | I | Blue data Bit3 (LSB). | 46 | G4FSC | | 4FSC/32FSC at PALCD-G. |
| 15 | OSDSW | I | OSD Enable/Disable. | 47 | GCLK | | Y-FILSEL THROU/FILON2 |
| 16 | CDGSWB | I | Select Video-CD(H)/CD-G(L). | 48 | YCDFF | | DAC (YOUT,COUT) OFF. |
| 17 | C4 | I | Blue data Bit4 (LSB). | 49 | YFILON | | Y-FILSEL THROU/FILON1 |
| 18 | C5 | I | Blue data Bit5 (LSB). | 50 | PAL60B | | Normal/pal60 at palmode. |
| 19 | C6 | I | Blue data Bit6 (LSB). | 51 | VCLK | I | Video clock input. |
| 20 | C7 | I | Blue data Bit7 (LSB). | 52 | RSTB | I | Normal / Reset. |
| 21 | GND | - | Digital Ground. | 53 | CLKSW | | SEL 1CLK/2CLK. |
| 22 | NTB | - | Select NTSC/PAL Mode. | 54 | RD0 | I | Red data Bit0 (LSB). |
| 23 | IM0 | I | Select YUV/RGB. | 55 | RD1 | I | Red data Bit1. |
| 24 | IM1 | I | Select DAC/NORMAL. | 56 | RD2 | I | Red data Bit2. |
| 25 | TEST1 | - | Normally pull down to GND. | 57 | ROSD | I | OSD red data input. |
| 26 | TEST2 | - | Select U/V timing. | 58 | RD3 | I | Red data Bit3. |
| 27 | CVSY | I/O | V-SYNC input or output. | 59 | RD4 | I | Red data Bit4. |
| 28 | HSY | I/O | H-SYNC input or output. | 60 | RD5 | I | Red data Bit5. |
| 29 | PIXCLK | - | 1/2freq of BCLK. | 61 | VDD | - | Digital VDD. |
| 30 | BLKB | O | Internal clock output. | 62 | RD6 | I | Red data Bit6. |
| 31 | VDD | - | Digital VDD. | 63 | RD7 | I | Red data Bit7. |
| 32 | INT | | Interalce/Non interlace | 64 | GOSD | I | OSD green data input. |

## ■BU2173F(IC105)

1.Terminal Layout




2.Block diagrams

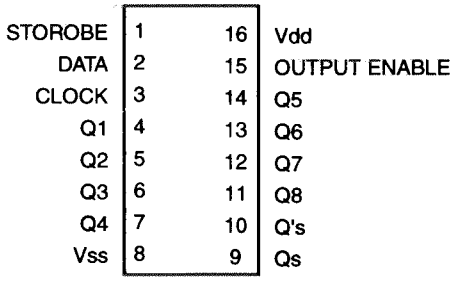



3.Pin function

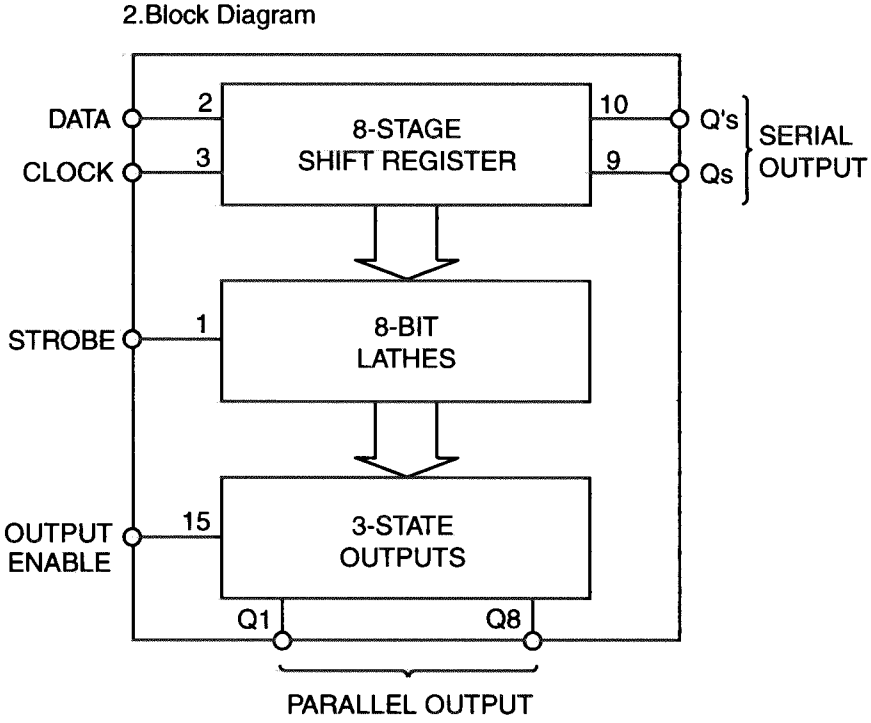
| Pin No. | Symbol | I/O | Function |
|---|---|---|---|
| 1 | VDD | - | Digital VDD. |
| 2 | TSTO | | Use open this pin for normal operation. |
| 3 | XTALI | I | Reference oscillation input. |
| 4 | XTALO | O | Reference oscillation output. |
| 5 | CTRLA | | Frequency select for V-CD/CD-G. |
| 6 | CTRLB | | Force H for normal operation. |
| 7 | CTRLC | | PAL/NTSC select for CD-G mode. |
| 8 | TSTI | | Force L for normal operation. |
| 9 | VSS | - | Digital GND. |
| 10 | AVSS | - | Analog GND. |
| 11 | FOUT3 | | Use open this pin for normal operation. |
| 12 | VSSIO | - | I/O GND. |
| 13 | FOUT2 | O | Clock output (2). |
| 14 | TEST | | Force L for normal operation. |
| 15 | FOUT1 | O | Clock output (1). |
| 16 | VDDIO | - | I/O VDD. |
| 17 | FOUT4 | O | Clock output (4). |
| 18 | AVDD | - | Analog VDD. |

## ■ BU4094BCF(IC304,IC303):SERIAL TO PARALLEL PROT EXTENSION

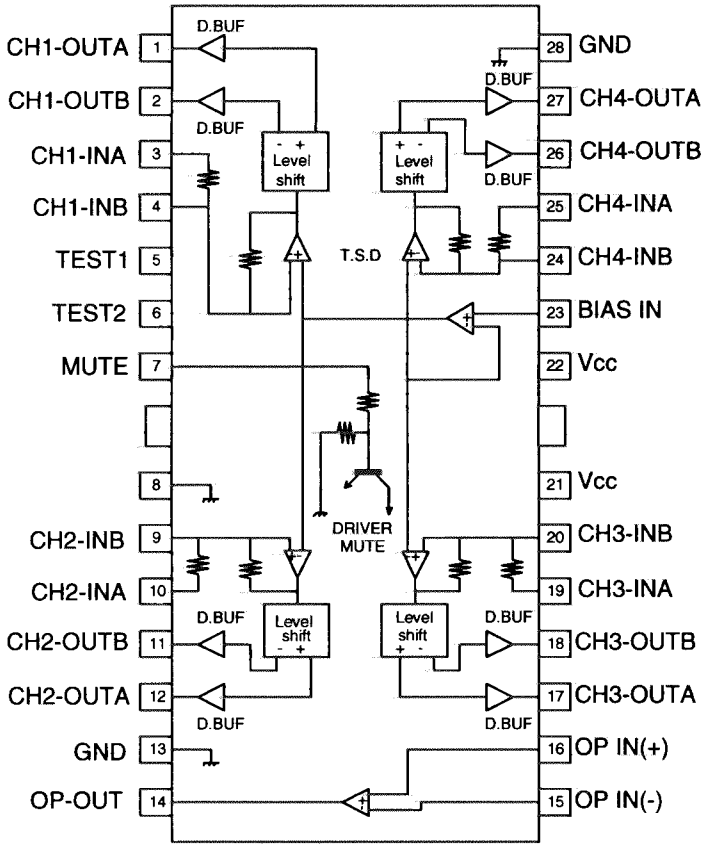
1.Terminal Layout




2.Block Diagram




## ■ BA6897FP-W(IC801):4channel driver

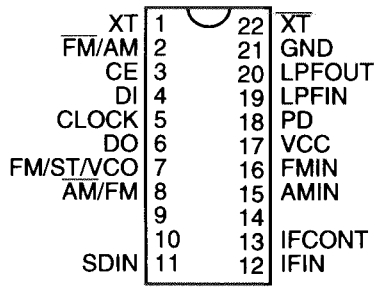


## ■CL480-F1(IC101):MPEG-1 AUDIO/VIDEO DECODER

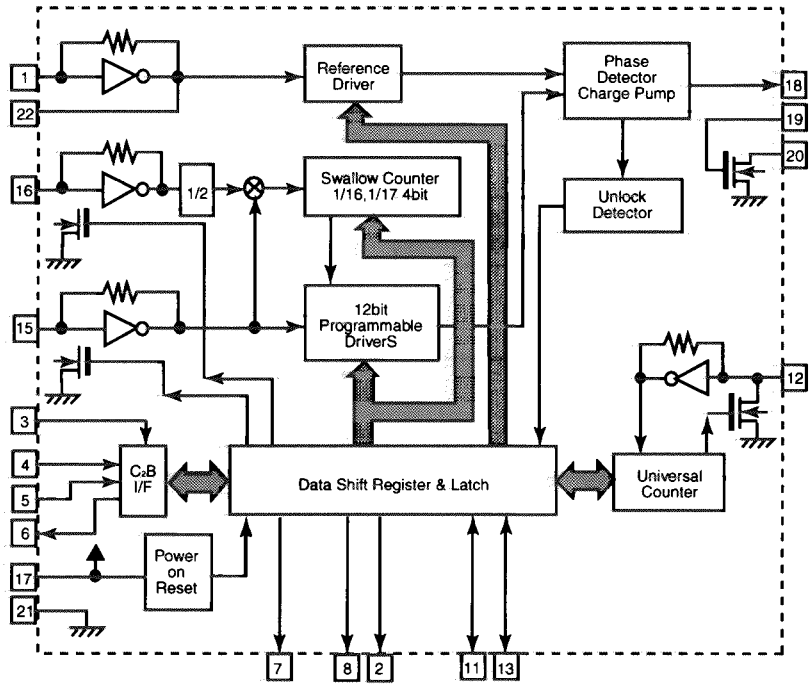
| Pin No. | Symbol | I/O | Function | Pin No. | Symbol | I/O | Function |
|---|---|---|---|---|---|---|---|
| 1 | HA2 | I | Host address. | 78~80 | VD10~12 | O | Video data terminal(G24/Y24) |
| 2 | DS | I | Data strobe terminal. | 81 | IOVDD | - | Power supply for Input/Output. |
| 3 | W/R | I | I/O read terminal. | 82~84 | VD13~15 | O | Video data terminal(G57/Y57) |
| 4 | IRQ | O | Interact terminal. | 85 | CKTVSS | - | Connect to GND. |
| 5 | DTACK | O | Acknowledge data output. | 86~89 | VD16~19 | O | Video data terminal(B0B3) |
| 6 | HD0 | I/O | Host data terminal. | 90 | IOVSS | - | Ground terminal for Input/Output. |
| 7 | IO VDD | - | Power supply for input/output. | 91~94 | VD20~23 | O | Video data terminal(B47) |
| 8,9 | HD1,2 | I/O | Host data terminal. | 95 | VSYNC | I/O | Vertical comparator/Composite |
| 10 | CKT VSS | - | Connected to GND. | | | | comparator output. |
| 11~15 | HD3~7 | I/O | Date data terminal. | 96 | HSYNC | I/O | Horizonatall synchronizing signal. |
| 16 | IOVSS | - | Ground terminal for Input/Output. | 97 | VOE | I | Video output enable signal. |
| 17 | TEST | I | Test terminal. | 98 | VCOVDD | - | Power supply of VCO. |
| 18 | XTLVSS | I | Oscillator ground terminal. | 99 | VCLK | I/O | Video clock terminal. |
| 19 | XTLIN | I | Oscillator input terminal. | 100 | VCOVSS | - | Ground of VCO. |
| 20 | XTLOUT | O | Oscillator output terminal. | 101 | RESET | I | Reset signal input. |
| 21 | XTLVDD | - | Power supply for oscillator. | 102 | IOVSS | - | Ground terminal for Input/Output. |
| 22 | CKTVDD | - | Power supply. | 103 | C2PO | I | Data error flag input. |
| 23~28 | MD0~5 | I/O | DRAM data / ROM data terminal. | 104 | CDLRCK | I | L/R word clock input. |
| 29 | IOVDD | - | Power supply for Input/Output. | 105 | CDDATA | I | Bit serial data input. |
| 30,31 | MD6,7 | I/O | DRAM data/ROM data terminal. | 106 | CDBCK | I | Bit clock output. |
| 32,33 | MCE01 | O | Chip enable output for ROM bank. | 107 | DALRCK | O | L/R clock output. |
| 34~37 | MD8~11 | I/O | DRAM data/ROM data terminal. | 108 | DADATA | O | Bit serial PCM audio signal output. |
| 38 | IOVSS | - | Ground terminal for Input/Output. | 109 | DABCK | O | Bit clock output. |
| 39~42 | MD12~15 | I/O | DRAM data/ROM address terminal. | 110 | IOVDD | - | Power supply for Input/Output. |
| 43 | 5VVDD | - | Power supply(+5V). | 111 | XCK | I | Bit clock input terminal. |
| 44 | LCAS | O | DRAM LCAS/ROM address terminal. | 112 | CKTVDD | - | Power supply. |
| 45 | LCASIN | I | DRAM LCAS input. | 113 | PIO12 | O | Interact 2 signal output. |
| 46 | CKTVSS | - | Connect to GND. | 114 | PIO11 | O | Non connect. |
| 47 | MWE | O | DRAM write enable signal output. | 115 | PIO10 | I | Host enable signal input. |
| 48 | UCAS | O | DRAM UCAS/ROM address terminal. | 116 | PIO9 | I | Boot ROM enable signal input. |
| 49 | IOVDD | - | Power supply for Input/Output. | 117 | PIO8 | O | Non connect. |
| 50 | UCASIN | | DRAM UCAS input terminal. | 118 | PIO7 | O | DAC emphasis signal output. |
| 51,52 | RAS0,1 | O | DRAM RAS0,1 terminal. | 119 | PIO6 | I | CD-DA emphasis signal output. |
| 53~57 | MA9~5 | O | DRAM data/ROM address terminal. | 120 | PIO5 | O | Non connect. |
| 58 | IOVSS | - | Ground terminal for Input/Output. | 121 | PIO4 | O | FMV detect signal output. |
| 59~63 | MA4~0 | O | DRAM data/ROM address terminal. | 122 | PIO3 | O | CD-DA video CD select signal |
| 64 | PIO0 | O | ROM address extension terminal. | | | | output Low:Video CD. |
| 65 | IOVDD | - | Power supply for Input/output. | 123 | 5VVDD | - | Power supply (+5V). |
| 66~72 | VD0~6 | O | Video data terminal | 124 | PIO2 | O | Non connect. |
| | | | (R6/CrCb6/YCrCb066) | 125 | IOVSS | - | Ground for Input/Output. |
| 73 | IOVSS | - | Ground terminal for Input/Output. | 126 | PIO1 | O | Non connect. |
| 74~76 | VD7~9 | O | Video data terminal | 127 | HA0 | - | Host address input. |
| | | | (R7/CrCb7/YCrCb7)(G0,1/Y0,1) | 128 | HA1 | - | Host address input. |
| 77 | CKTVDD | - | Power supply. | | | | |

## ■ LC72136N(IC2):PLL Frequency sinsesizer L S I

1. Layout




2. Block

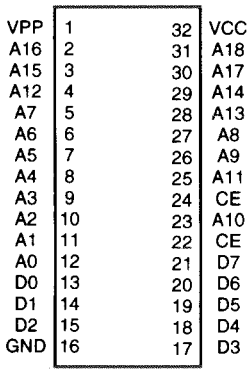



3. Function

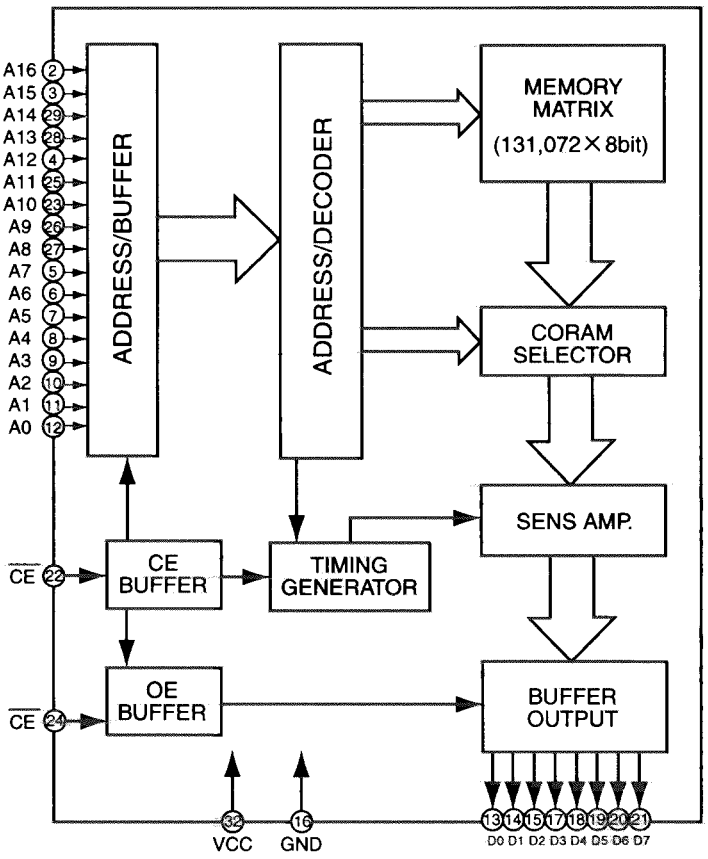
| Pin No. | Symbol | I/O | Function | Pin No. | Symbol | I/O | Function |
|---|---|---|---|---|---|---|---|
| 1 | XT | I | X'tal oscillator connect (75KHz) | 12 | IFIN | I | IF counter signal input |
| 2 | $\overline{FM}$/AM | O | LOW:FM mode | 13 | IFCONT | O | IF signal output |
| 3 | CE | I | When data output/input for 4pin(input) and 6pin(output): H | 14 | | - | Not use |
| 4 | DI | I | Input for receive the sirisl data from controller | 15 | AMIN | I | AM Local OSC signal output |
| 5 | CLOCK | I | Sync signal input use | 16 | FMIN | I | FM Local OSC signal input |
| 6 | DO | O | Data output for Controller Output port | 17 | VCC | - | Power suplly(VDD=4.5~5.5V) When power ON:Reset circuit move |
| 7 | FM/ST/VCO | O | "Low": MW mode | 18 | PD | O | PLL charge pump output(H: Local OSC frequency Height than Reference frequency. L: Low Agreement: Height impedance) |
| 8 | AM/FM | O | Not use | 19 | LPFIN | I | Input for active lowpassfilter of PLL |
| 9 | — | - | Not use | 20 | LPFOUT | O | Output for active lowpassfilter of PLL |
| 10 | | - | Input/output port | 21 | GND | - | Connected to GND |
| 11 | SDIN | I/O | Data input/output | 22 | $\overline{XT}$ | I | X'tal oscillator(75KHz) |

## ■LH531HEG(IC102)

1.Terminal Layout




2.Block diagram

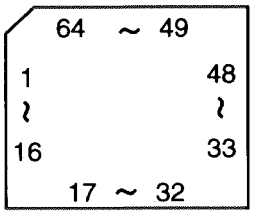



3.Pin Function

| Pin No. | Symbol | I/O | Function |
|---|---|---|---|
| 1 | VPP | - | Power supply. |
| 2 | A16 | I | Adress input. |
| 3 | A15 | I | Adress input. |
| 4 | A12 | I | Adress input. |
| 5~12 | A7A0 | I | Adress input. |
| 13~15 | D0D2 | O | Data output. |
| 16 | GND | - | Connect to GND |
| 17~21 | D3D7 | O | Data output. |
| 22 | CE | I | Chip enable input. |
| 23 | A10 | I | Adress input. |
| 24 | CE | I | Chip enable input. |
| 25 | A11 | I | Adress input. |
| 26,27 | A9,A8 | I | Adress input. |
| 28,29 | A13,A14 | I | Adress input. |
| 30,31 | D17,D18 | O | Data output. |
| 32 | VCC | - | Power supply. |

## ■MN171601AK8J2(IC111):HOST Micro Computer

1.Terminal Layout

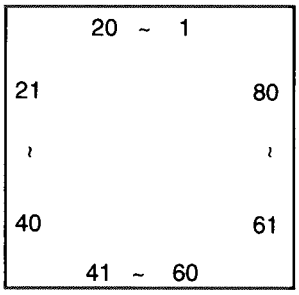



2.Pin Function

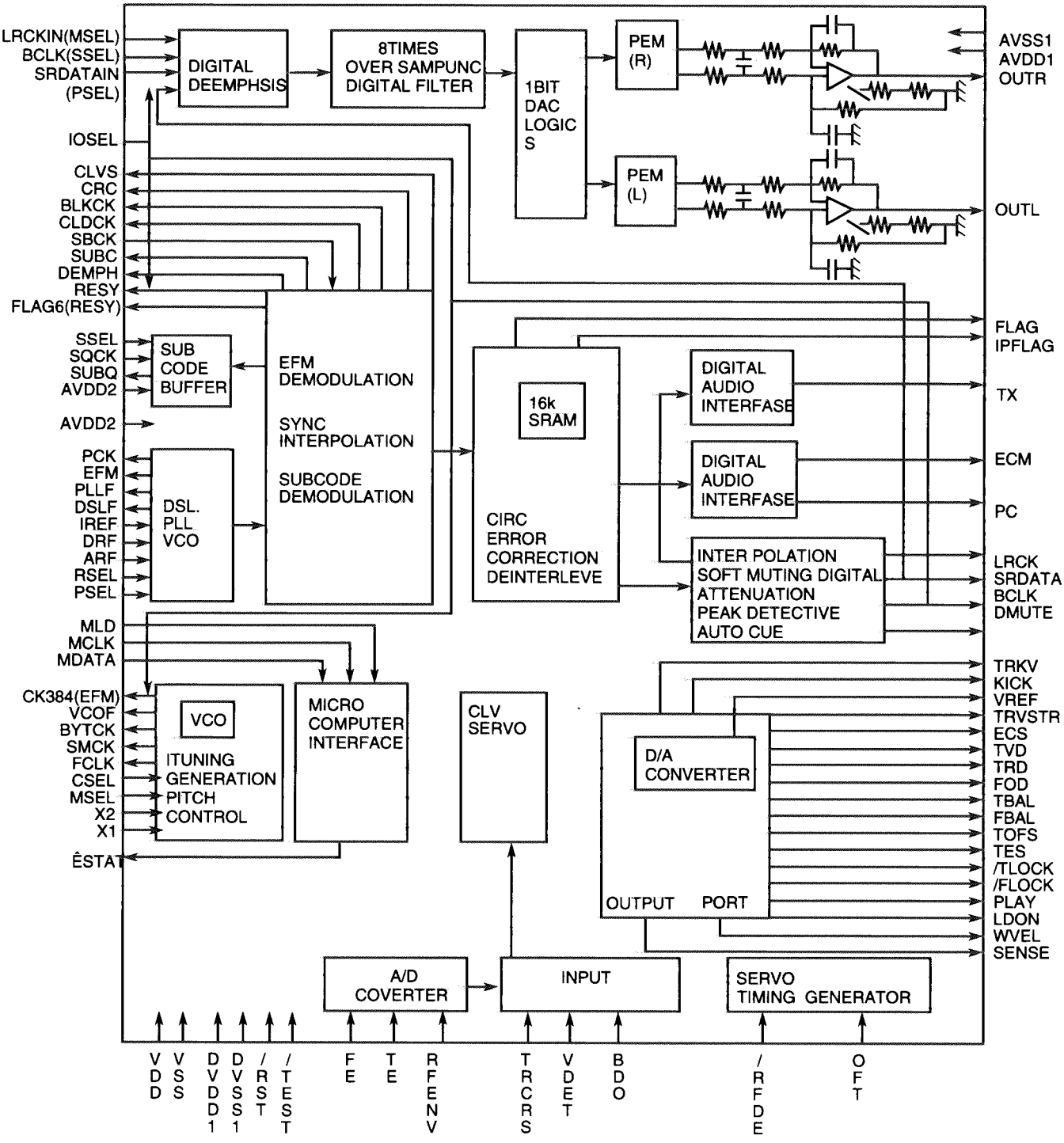
| Pin No. | Symbol | I/O | Function |
|---|---|---|---|
| 1 | 480RST | O | Reset signal output. |
| 2 | MREQ | I | Input the transfer request data signal. |
| 3 | ACTINT | I | Interact 2 signal input. |
| 4 | GDET | I | CD-G detect terminal H:CD-G |
| 5 | GND | - | Connected to GND. |
| 6 | DTACK | I | Acknowledge signal input. |
| 7 | GND | - | Connect to GND. |
| 8 | GND | - | Connect to GND. |
| 9 | DIR | I/O | Input/Output control for IC114. |
| 10 | N/PAL | - | Not use. |
| 11 | RGB | O | Video out control signal (H:RGB L:composite) |
| 12 | W/R | I/O | Read/Write signal input/output. |
| 13~15 | HA02 | O | Address signal output for MPEG LSI. |
| 16 | DS | O | Data strobe signal output. |
| 17~24 | HD07 | I/O | Data terminal for MPEG LSI. |
| 25~39 | SA014 | O | SRAM address signal output. |
| 40 | SCS | O | SRAM chip select signal output. |
| 41~48 | SD18 | I/O | SRAM data Input/Output terminal. |
| 49 | SR/W | I/O | SRAM read/write signal input/output. |
| 50 | PAL60 | - | Not use. |
| 51 | RESET | I | Reset signal input. |
| 52 | X1 | - | Non connect |
| 53 | X2 | - | Non connect. |
| 54 | VSS | - | Connect to GND. |
| 55 | OSC2 | - | Non connect. |
| 56 | OSC1 | I | Clock input terminal. |
| 57 | VDD | - | Power supply. |
| 58 | HREQ | O | Communication signal output. |
| 59 | SRCLK | O | Clock signal for data request. |
| 60 | M2HDT | O | Serial data output. |
| 61 | M2MDT | I | Serial data input. |
| 62 | HRDY | O | Communication signal output. |
| 63 | VCD/G | O | Video swith switching signal output. |
| 64 | PALCDG | O | CD-G PAL/NTSC clock select terminal. |

## ■ MN35510(IC651):DIGITAL SERVO&DIGITAL SIGNAL PROCESSER

1. Terminal Layout




2.Block Diagram

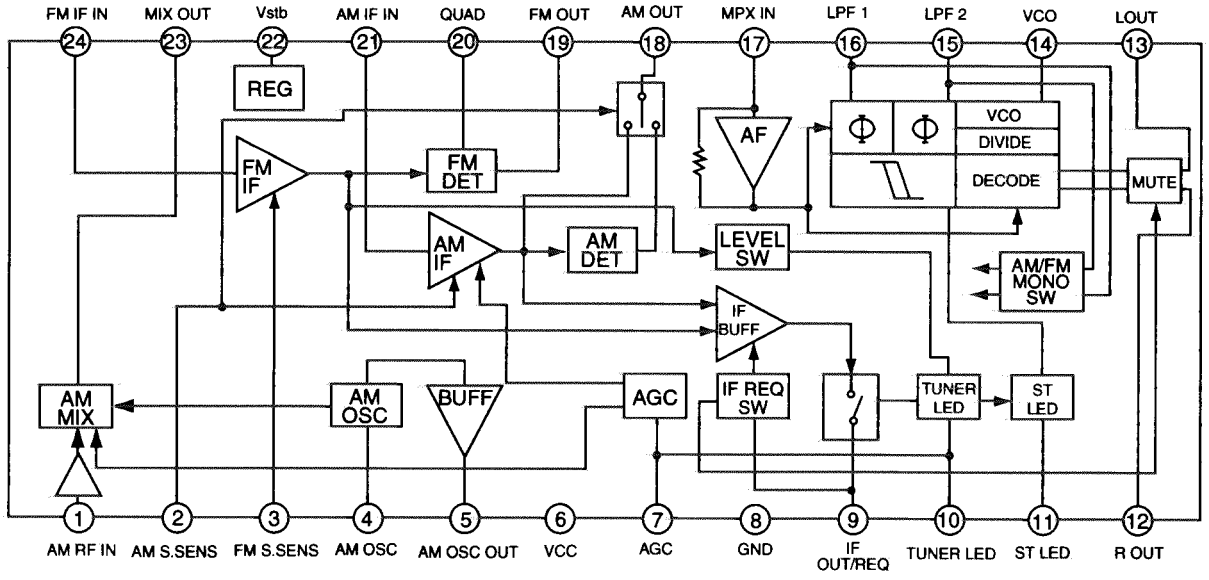


## 3. Description

| Pin No. | symbol | I/O | Description | Pin No. | symbol | I/O | Description |
|---|---|---|---|---|---|---|---|
| 1 | BCLK | O | Not used | 41 | TES | O | Tracking error shunt signal output(H:shunt) |
| 2 | LRCK | O | Not used | 42 | PLAY | – | Not used |
| 3 | SRDATA | O | Not used | 43 | WVEL | – | Not used |
| 4 | DVDD1 | – | Power supply (Digital) | 44 | ARF | I | RF signal input |
| 5 | DVSS1 | – | Connected to GND | 45 | IREF | I | Reference current input pin |
| 6 | TX | O | Digital audio interface output | 46 | DRF | I | Bias pin for DSL |
| 7 | MCLK | I | μcom command clock signal input (Data is latched at signal's rising point) | 47 | DSLF | I/O | Loop filter pin for DSL |
| 8 | MDATA | I | μcom command data input | 48 | PLLF | I/O | Loop filter pin for PLL |
| 9 | MLD | I | μcom command load signal input | 49 | VCOF | – | Not used |
| 10 | SENSE | O | Sence signal output | 50 | AVDD2 | – | Power supply(Analog) |
| 11 | FLOCK | O | Focus lock signal output Active :Low | 51 | AVSS2 | – | Connected to GND(Analog) |
| 12 | TLOCK | O | Tracking lock signal output Active :Low | 52 | EFM | – | Not used |
| 13 | BLKCK | O | sub-code·block·clock signal output | 53 | PCK | – | Not used |
| 14 | SQCK | I | Outside clock for sub-code Q resister input | 54 | PDO | – | Not used |
| 15 | SUBQ | O | Sub-code Q -code output | 55 | SUBC | – | Not used |
| 16 | DMUTE | – | Connected to GND | 56 | SBCK | – | Not used |
| 17 | STATUS | O | Status signal (CRC,CUE,CLVS,TTSTOP,ECLV,SQOK) | 57 | VSS | – | Connected to GND(for X'tal oscillation circuit) |
| 18 | RST | I | Reset signal input (L:Reset) | 58 | XI | I | Input of 16.9344MHz X'tal oscillation circuit |
| 19 | SMCK | – | Not used | 59 | X2 | O | Output of X'tal oscillation circuit |
| 20 | PMCK | – | Not used | 60 | VDD | – | Power supply(for X'tal cscillation circuit) |
| 21 | TRV | O | Traverse enforced output | 61 | BYTCK | – | Not used |
| 22 | TVD | O | Traverse drive output | 62 | CLDCK | – | Not used |
| 23 | PC | – | Not used | 63 | FLAG | – | Not used |
| 24 | ECM | O | Spindle motor drive signal (Enforced mode output) 3-State | 64 | IPPLAG | – | Not used |
| 25 | ECS | O | Spindle motor drive signal (Servo error signal output) | 65 | FLAG | – | Not used |
| 26 | KICK | O | Kick pulse output | 66 | CLVS | – | Not used |
| 27 | TRD | O | Tracking drive output | 67 | CRC | – | Not used |
| 28 | FOD | O | Focus drive output | 68 | DEMPH | | Not used |
| 29 | VREF | I | Reference voltage input pin for D/A output block (TVD,FOD,FBA,TBAL) | 69 | RESY | – | Not used |
| 30 | FBAL | O | Focus Balance adjust signal output | 70 | IOSEL | – | pull up |
| 31 | TBAL | O | Tracking Balance adjust signal output | 71 | TEST | – | pull up |
| 32 | FE | I | Focus error signal input(Analog input) | 72 | AVDD1 | – | Power supply(Digital) |
| 33 | TE | I | Tracking error signal input(Analog input) | 73 | OUT L | O | Lch audio output |
| 34 | RF ENV | I | RF envelope signal input(Analog input) | 74 | AVSS1 | – | Connected to GND |
| 35 | VDET | I | Vibration detect signal input(H:detect) | 75 | OUT R | O | Rch audio output |
| 36 | OFT | I | Off track signal input(H:off track) | 76 | RSEL | – | pull up |
| 37 | TRCRS | I | Track cross signal input | 77 | CSEL | – | Connected to GND |
| 38 | RFDET | I | RF detect signal input(L:detect) | 78 | PSEL | – | Connected to GND |
| 39 | BDO | I | BDO input pin(L:detect) | 79 | MSEL | – | Connected to GND |
| 40 | LDON | O | Laser ON signal output(H:on) | 80 | SSEL | – | Pull up |

## ■ TA2057N(IC1):FM/AM IF AMP & Detector

### 1.Block Diagrams

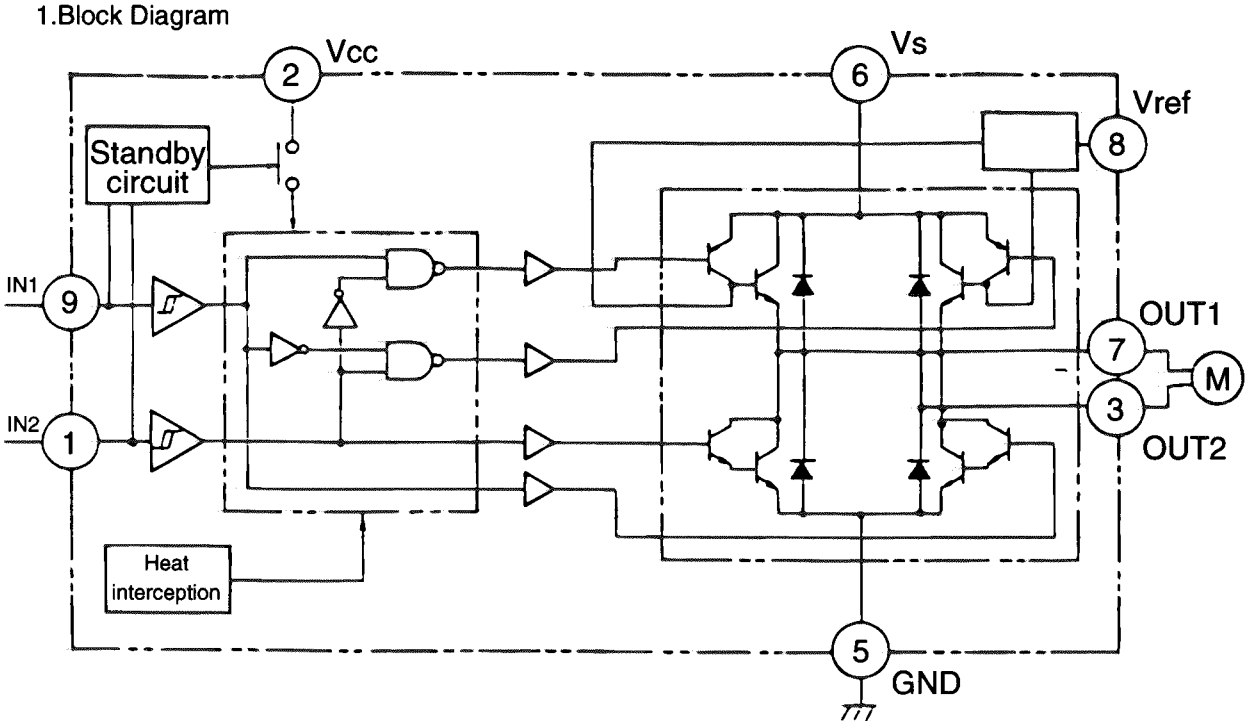



### 2.Pin Function

| Pin No. | I/O | Symbol | Function | Pin No. | I/O | Symbol | Function |
|---|---|---|---|---|---|---|---|
| 1 | I | AM RF | AMRF signal input | 13 | O | Lch OUT | Output Lch |
| 2 | | AM S.SENS | | 14 | O | VCO | Voltage controlled terminal |
| 3 | | FM S.SENS | | 15 | O | LPF2 | When voltage of terminal is MONO |
| 4 | - | AM OSC | AM local oscillation circuit | | | | at "H" and ST at "L" |
| 5 | O | AM OSC OUT | AM local oscillation signal output | 16 | O | LPF1 | When voltage of terminal is AM at |
| 6 | - | VCC | Power supply | | | | "H" and FM at "L" |
| 7 | I | AGC | AGC voltage input terminal | 17 | I | MPX IN | Multi plex signal input |
| 8 | - | GND | Connect to GND | 18 | O | AM OUT | AM detection signal output |
| 9 | O | IF OUT | IF REQ signal output to IC2 | 19 | O | FM OUT | FM detection signal output |
| 10 | O | TU IND | Indicator drive output when tuning | 20 | I | FM QUAD | Bypass to FMIF |
| 11 | O | ST IND | Stereo indicator output | 21 | I | AM IF IN | Input of AMIF signal |
| | | | "H"mono . "L"stereo | 22 | - | Vst | Fixed voltage output terminal |
| 12 | O | Rch OUT | Output Rch | 23 | O | AM MIX OUT | Output terminal for AM mixer |
| | | | | 24 | I | FM IF IN | Input of FMIF signal |

## ■TA8409S(IC851.IC852):Motor Driver

1.Block Diagram



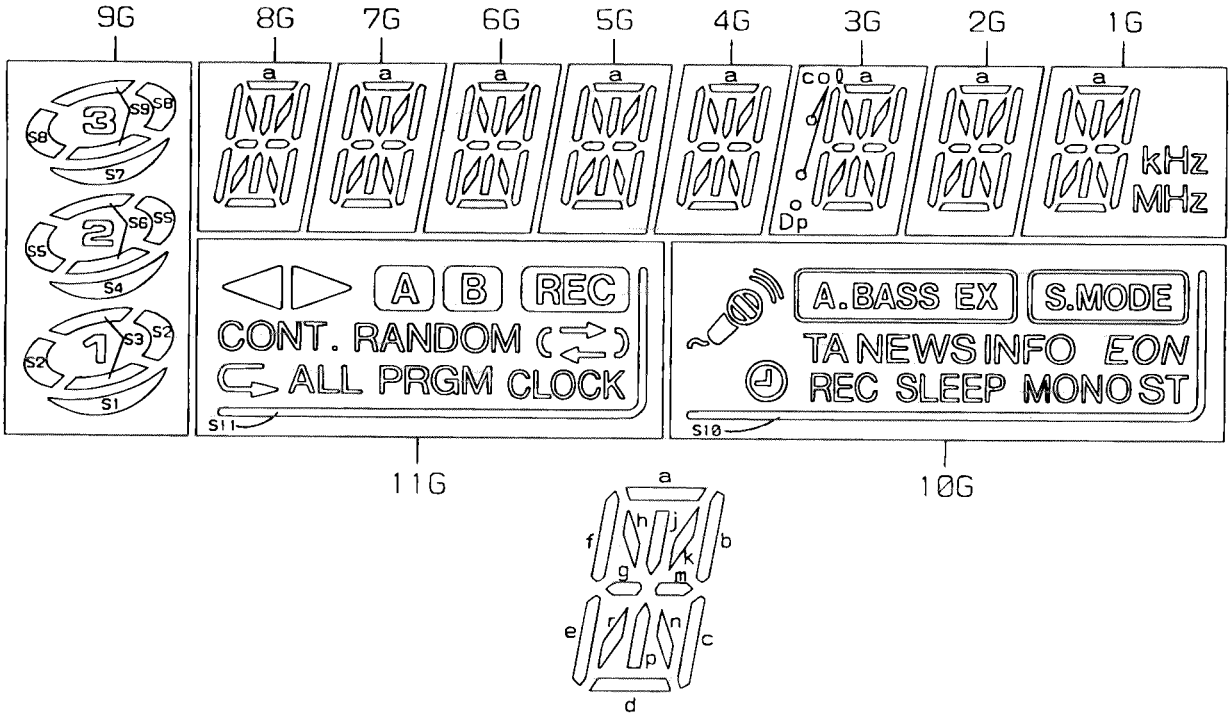

2.Function

| INPUT | | OUTPUT | | MODE |
|---|---|---|---|---|
| IN1 | IN2 | OUT1 | OUT2 | MOTOR |
| 0 | 0 | ∞ | ∞ | STOP |
| 1 | 0 | H | L | CW/CCW |
| 0 | 1 | L | H | CCW/CW |
| 1 | 1 | L | L | BRAKE |

# Internal Connections for FL Display Tube

## ■QLF0047-001(FL701)

Grid Assignment






(8G~1G)

ANODE CONNECTION

| | 11G | 10G | 9G | 8G | 7G | 6G | 5G | 4G | 3G | 2G | 1G |
|---|---|---|---|---|---|---|---|---|---|---|---|
| P1 | ◁ | | 1 | d | d | d | d | d | d | d | d |
| P2 | ▷ | | S1 | n | n | n | n | n | n | n | n |
| P3 | A | (A.BASS.EX) | S2 | p | p | p | p | p | p | p | p |
| P4 | B | A.BASS EX | S3 | r | r | r | r | r | r | r | r |
| P5 | REC | (S.MODE) | 2 | e | e | e | e | e | e | e | e |
| P6 | CONT. | S.MODE | S4 | c | c | c | c | c | c | c | c |
| P7 | RANDOM | | S5 | g | g | g | g | g | g | g | g |
| P8 | ( | TA | S6 | m | m | m | m | m | m | m | m |
| P9 | ⇄ | NEWS | 3 | f | f | f | f | f | f | f | f |
| P10 | ) | INFO | S7 | b | b | b | b | b | b | b | b |
| P11 | ⊂ | EON | S8 | k | k | k | k | k | k | k | k |
| P12 | ALL | REC | S9 | j | j | j | j | j | j | j | j |
| P13 | PRGM | SLEEP | - | h | h | h | h | h | h | h | h |
| P14 | CLOCK | MONO | - | a | a | a | a | a | a | a | a |
| P15 | S11 | ST | - | - | - | - | - | - | col | - | kHz |
| P16 | - | S10 | - | - | - | - | - | - | Dp | - | MHz |

# Self Diagnosis Function of CD

## 1. Purpose

This function is designed to display an error to readily clarify the cause of such an error should any trouble occur in CD.

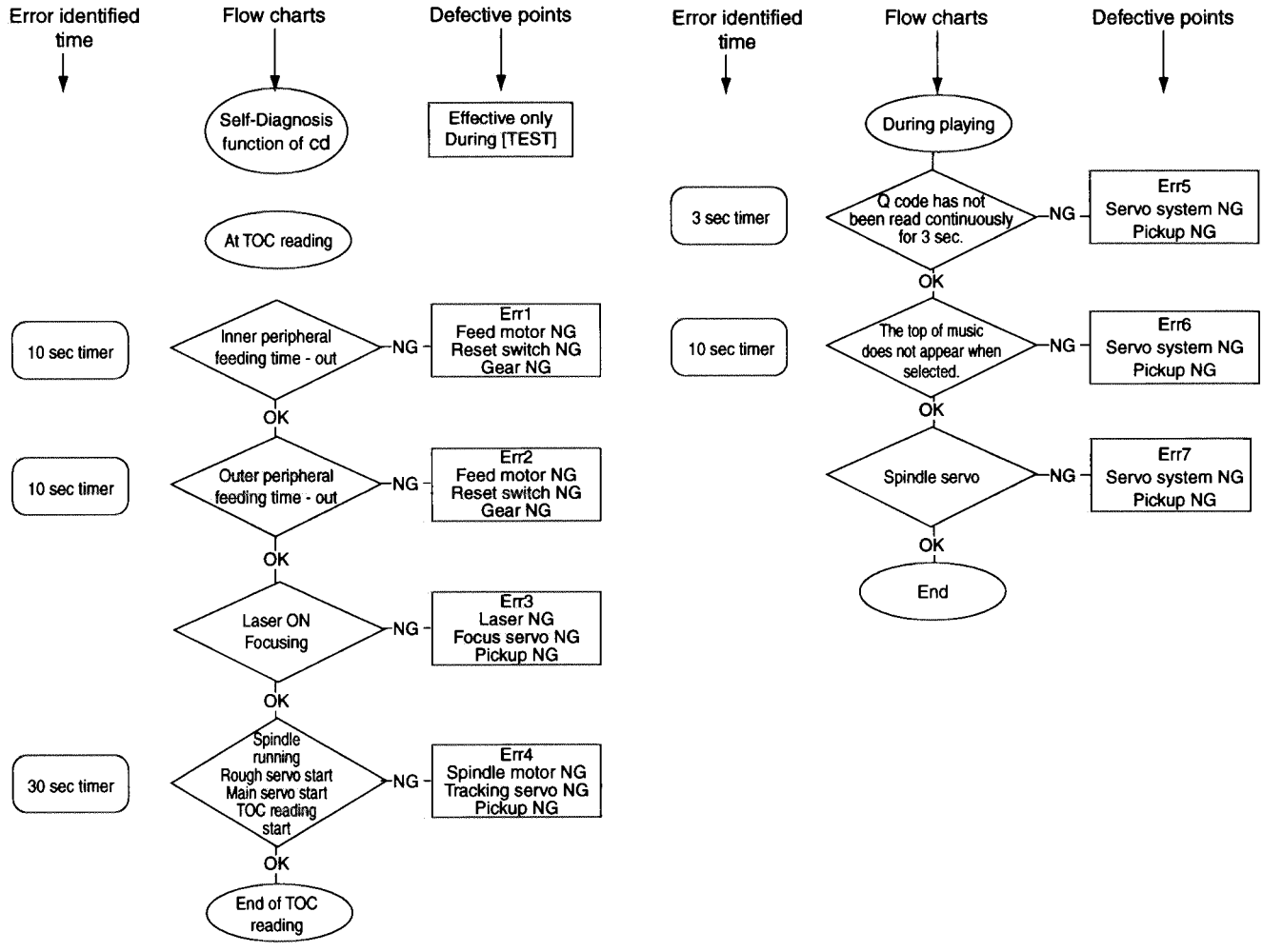
## 2. How to Use the Function

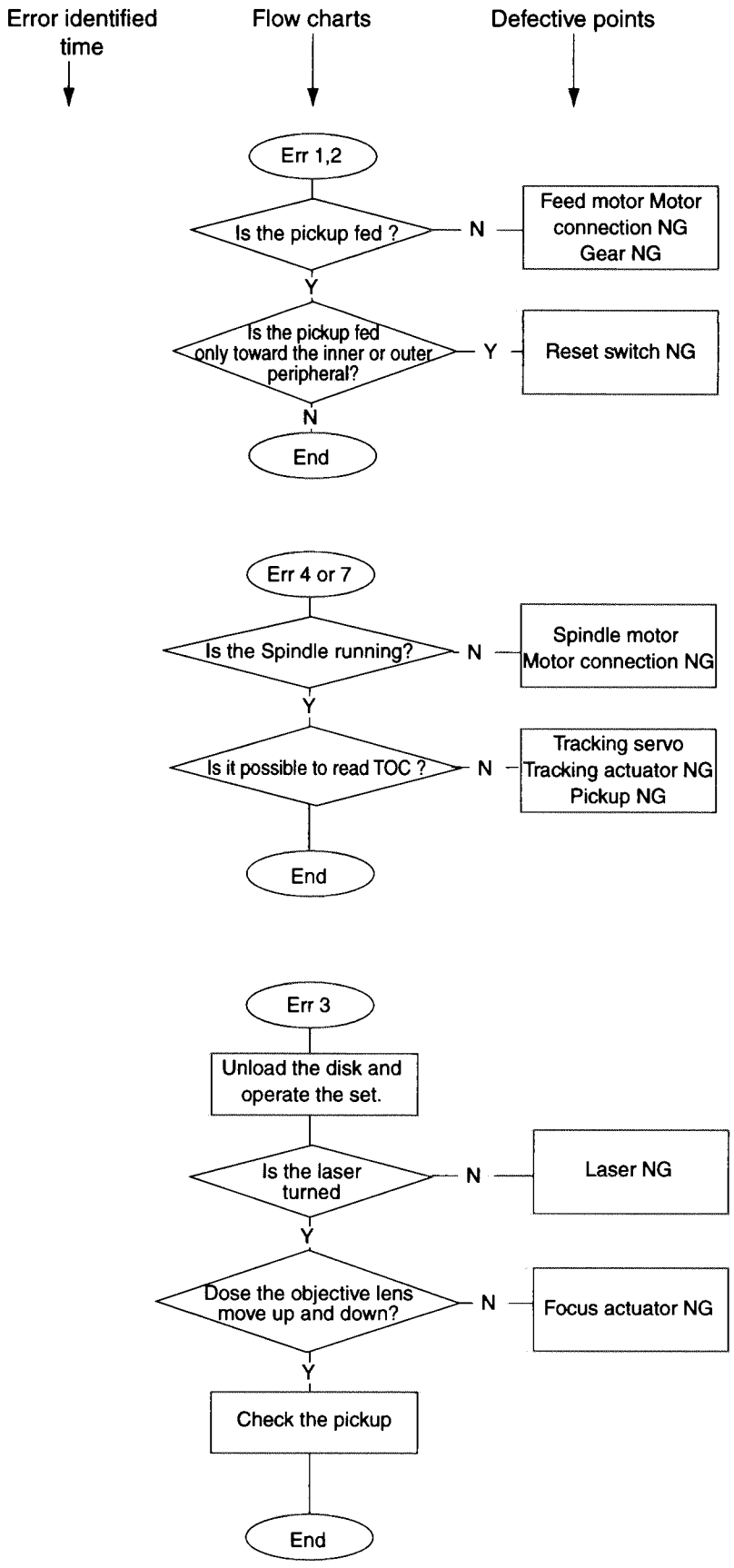
(1) Turn the microcomputer action of the set to [TEST] mode.

(2) Press CDSTOP + +10 + POWER on the remote control same time. Confirm that all of the LCDs have been turned on when set to the [TEST] mode subsequent to the step in item (2).

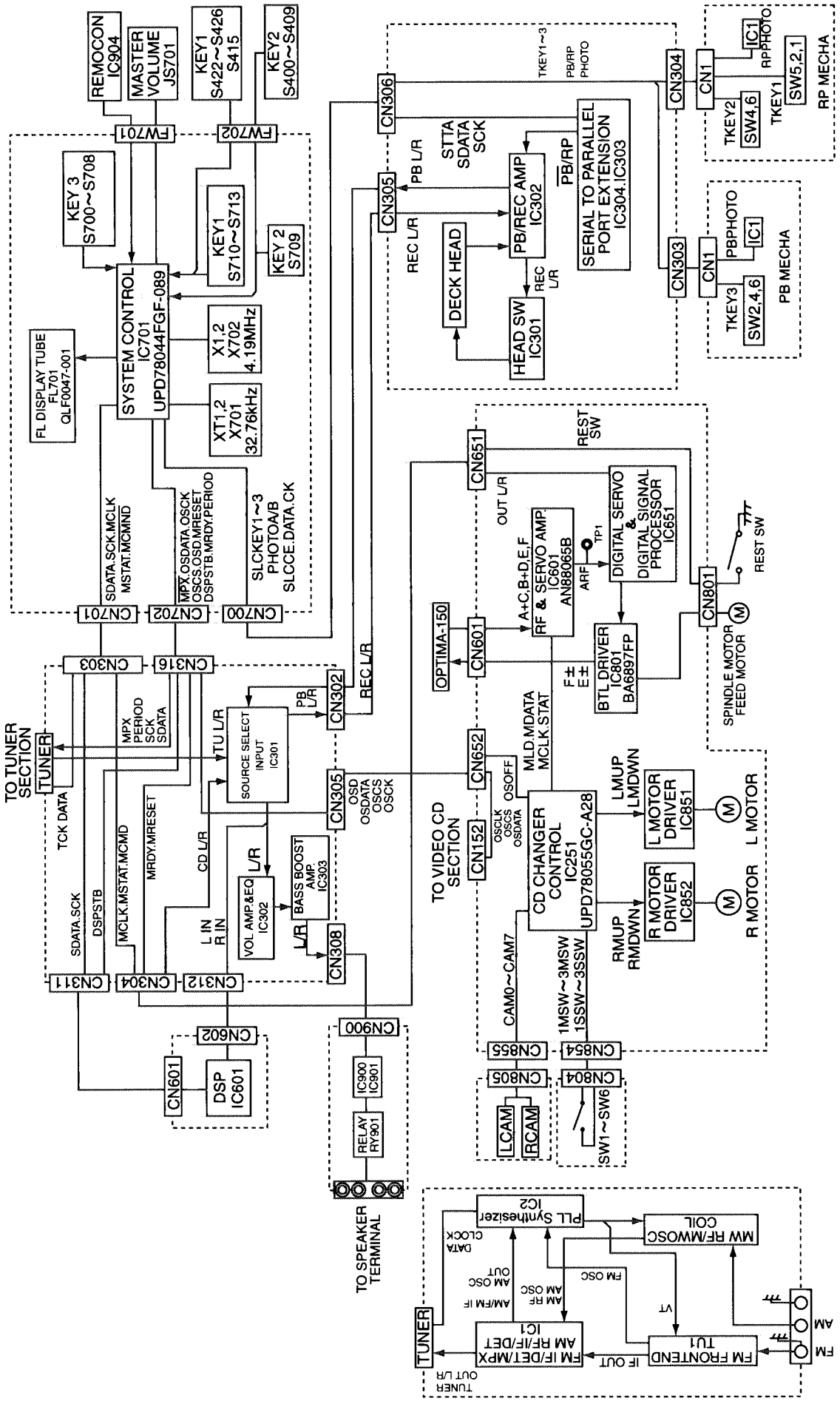
(3) When the CD trouble has occurred after starting CD, an error code will be displayed on the display section of LCD, etc.

## 3. Error code and location in trouble



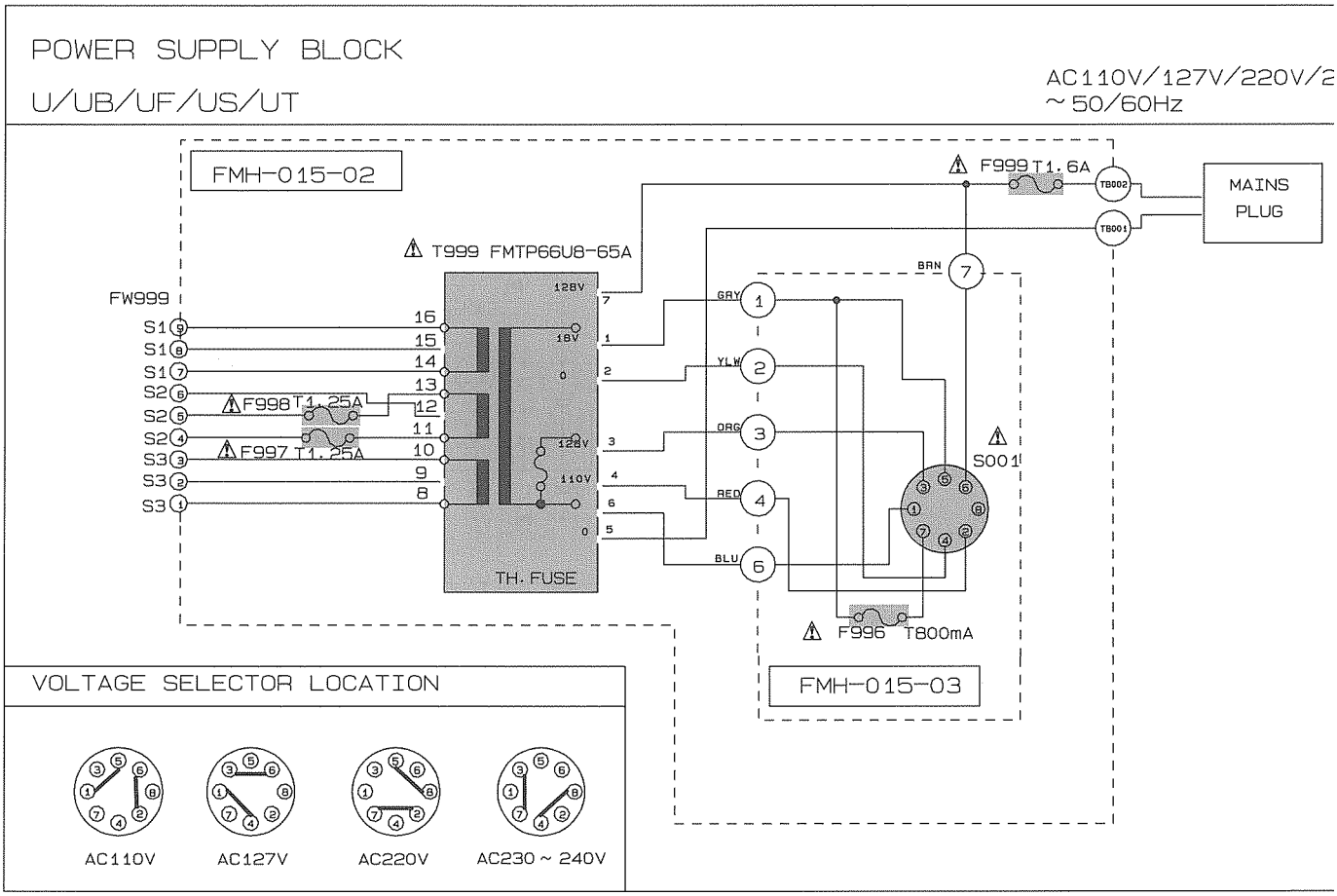

Error identified time
Flow charts
Defective points
Err 1,2
Is the pickup fed ?
N
Feed motor Motor connection NG Gear NG
Y
Is the pickup fed only toward the inner or outer peripheral?
Y
Reset switch NG
N
End
Err 4 or 7
Is the Spindle running?
N
Spindle motor Motor connection NG
Y
Is it possible to read TOC ?
N
Tracking servo Tracking actuator NG Pickup NG
End
Err 3
Unload the disk and operate the set.
Is the laser turned
N
Laser NG
Y
Dose the objective lens move up and down?
N
Focus actuator NG
Y
Check the pickup
End

## ■Block Diagrams



# Standard Schematic Diagram

## Power Transformer Section



VERSION CODES

UB : HONG KONG

UF : CHINA

US : SINGAPORE

UT : TAIWAN

U : UNIVERSAL EXCEPT ALL OF ABOVES

20V/230V-240V

INS
UG

AC110V/127V/
220V/230V-240V
~ 50/60HZ

| EXPLANATION OF OVERALL SCHEMATIC |
|---|
| MODEL : MX-V508T AND MX-V588T |

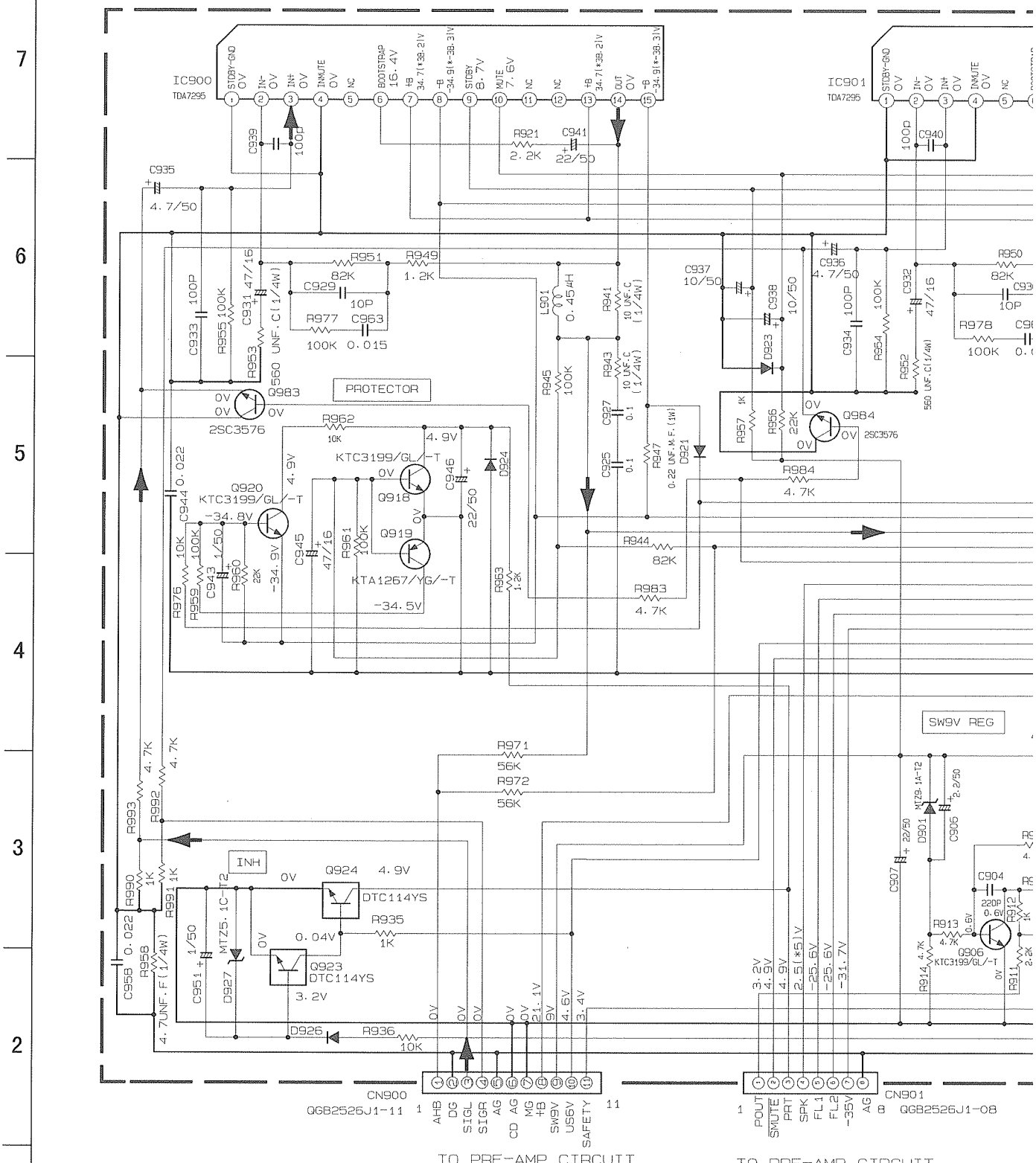
| SHEET NUMBER | MODEL NUMBER | CIRCUITS DESCRIPTION |
|---|---|---|
| 1/10 | MX-V508T MX-V588T | PRIMARY CIRCUIT |
| 2/10 | MX-V508T MX-V588T | POWER AMP CIRCUIT |
| 3/10 | MX-V508T MX-V588T | PRE-AMP CIRCUIT |
| 4/10 | MX-V508T MX-V588T | MICON & FL DISPLAY CIRCUIT |
| 5/10 | MX-V508T MX-V588T | MIC & HEADPHONE |
| 6/10 | MX-V508T MX-V588T | KARAOKE CONTROL CIRCUIT [DSP] |
| 7/10 | MX-V508T MX-V588T | CASSETE MECHA CONTROL CIRCUIT [SLC] |
| 8/10 | MX-V508T MX-V588T | TUNER CONTROL CIRCUIT |
| 9/10 | MX-V508T MX-V588T | VIDEO CD CONTROL CIRCUIT |
| 10/10 | MX-V508T MX-V588T | CD CONTROL & SERVO CIRCUIT [VC3] |

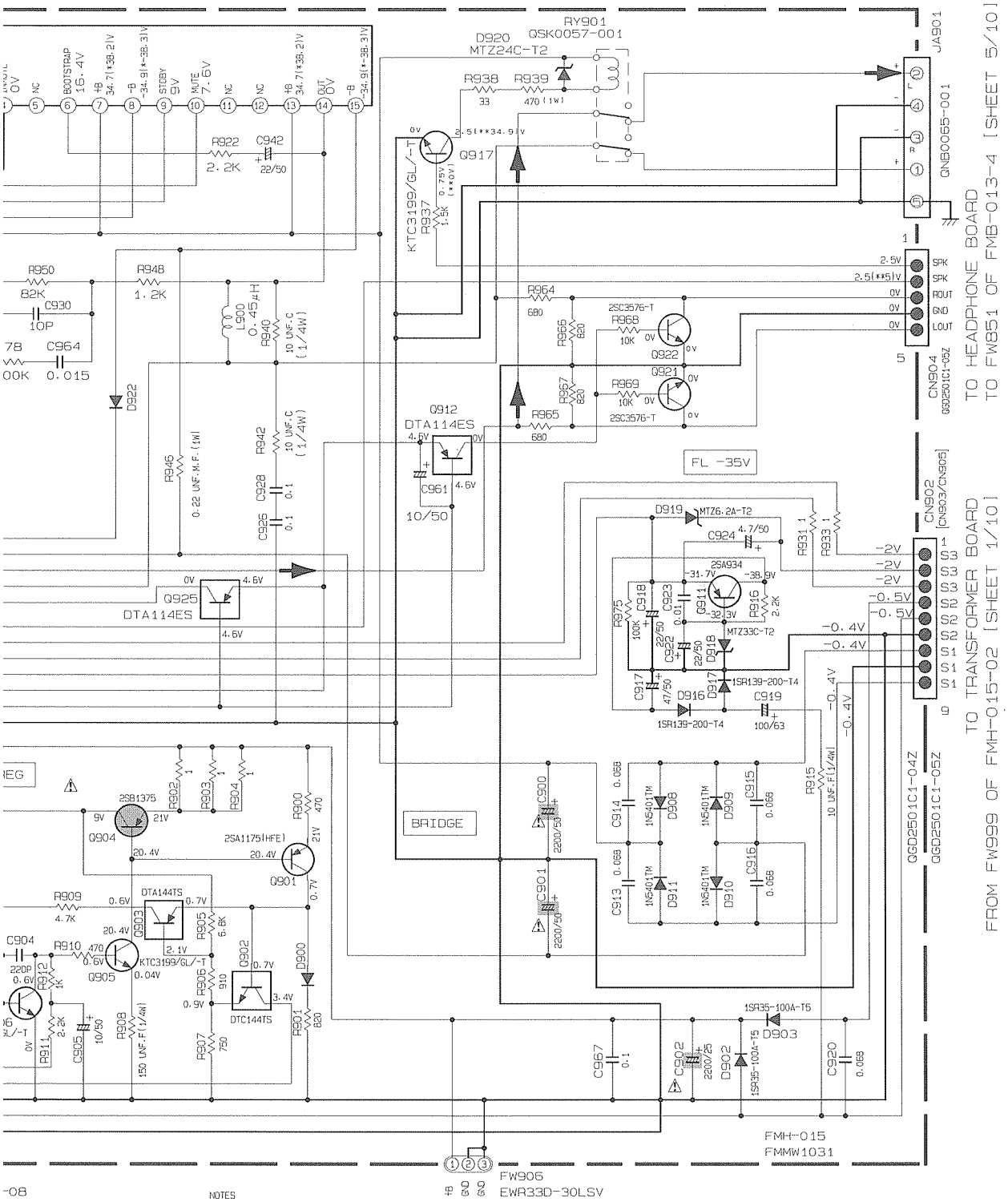
MODEL
MX-V508T/MX-V588T

⚠ Parts are safety assurance parts.
When replacing those parts make
sure to use the specified one.

| F | G | H | I | J |
|---|---|---|---|---|

## Power Amplifier & Regulator Section






NOTES

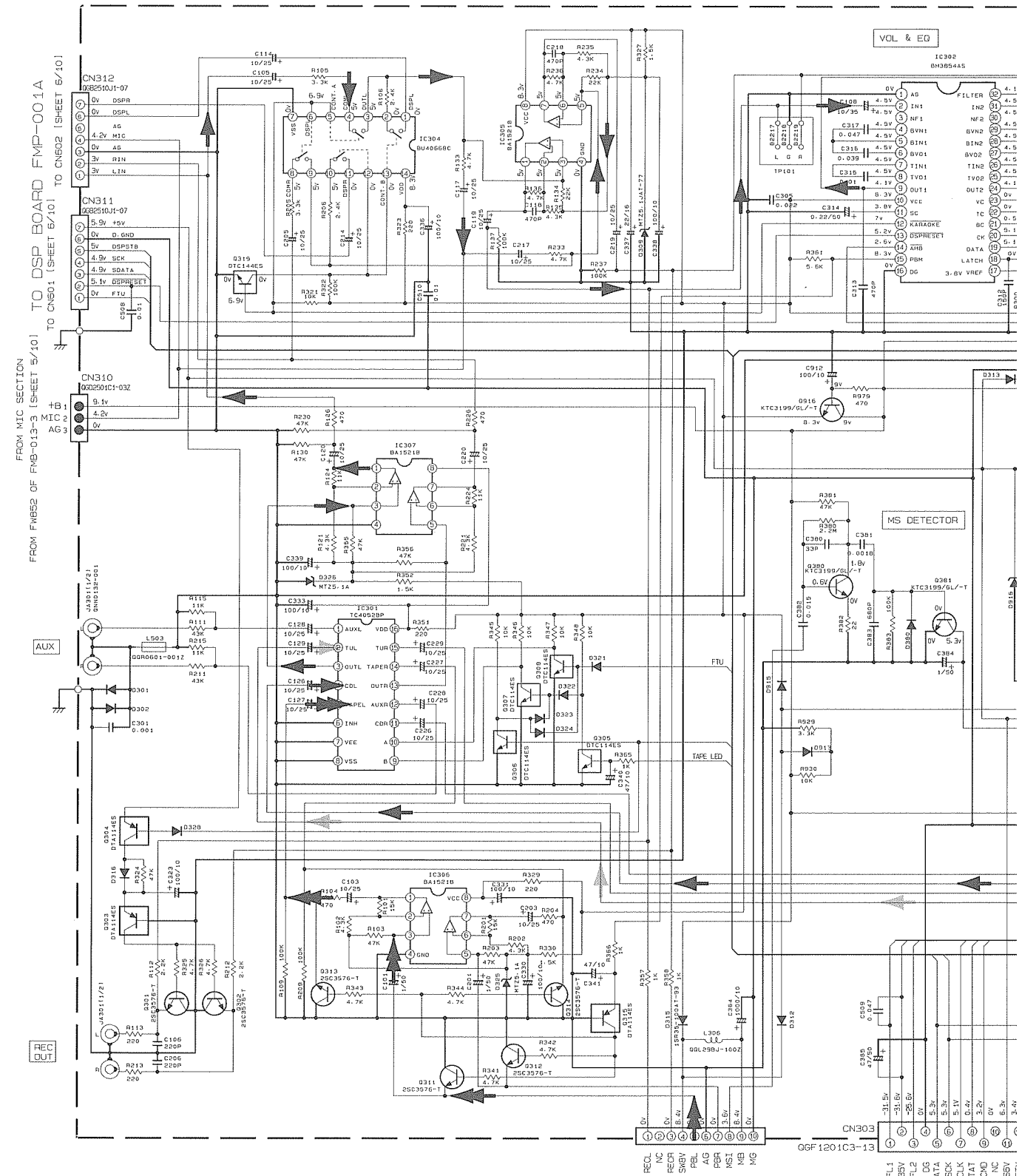
1. VOLTAGES ARE DC-MEASURED USING A DIGITAL VOLTMETER OR AN OSCILLOSCOPE WITHOUT INPUT SIGNAL CONDITION
   VOLTAGE VALUE MARKED * IS FOR J VERSION.
   VOLTAGE VALUE MARKED ** IS IN HEADPHONE POSITION.
2. UNLESS OTHERWISE SPECIFIED
   ALL RESISTORS ARE 1/4W ± 5% CARBON RESISTOR.
   ALL CAPACITORS ARE 50V CERAMIC CAPACITOR OR 50V MYLAR CAPACITOR.
   ALL RESISTANCE VALUES ARE IN OHM(Ω).
   ALL CAPACITANCE VALUES ARE IN μF(P=pF).
   ALL E.CAPACITORS ARE SHOWN IN THE FORM OF CAPACITANCE(μF)/RATED VOLTAGE (V).
   ALL DIODES ARE 1SS133T-77 TYPE
   (PP) POLYPROPYLENE CAPACITOR
   (M) 50V ± 5% MYLAR CAPACITOR OR 50V ±5% THIN FILM CAPACITOR
3. THOSE PART WITH BRACKET IS NOT USED.
   FOR RESISTOR, IT WOULD BE A SHORT.
   FOR CAPACITOR, IT WOULD BE AN OPEN.

⚠ Parts are safety assurance parts. When replacing those parts make sure to use the specified one.

MAIN SIGNAL

| F | G | H | I | J |
|---|---|---|---|---|

# Function & Main Amplifier Section

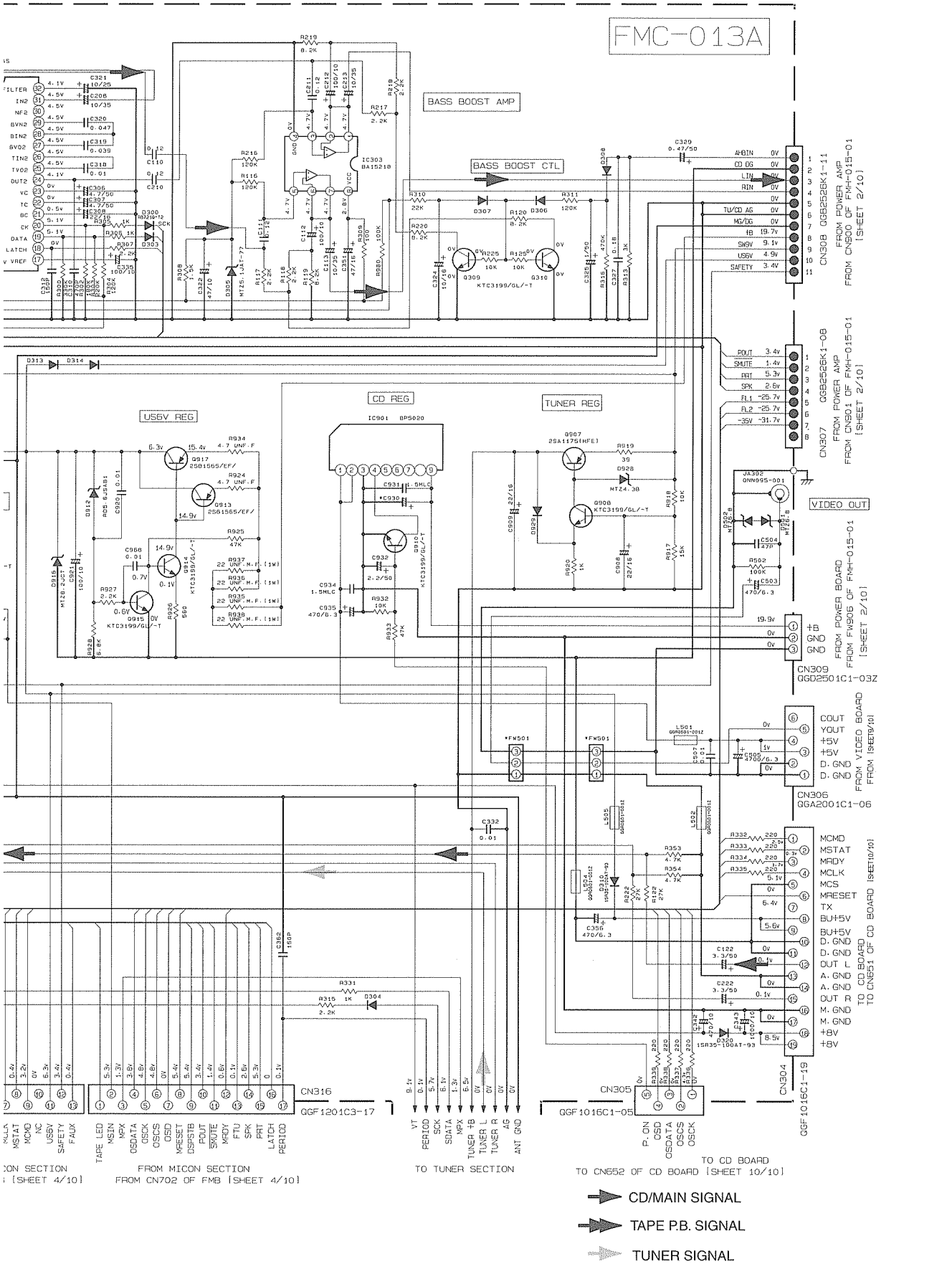



NOTES

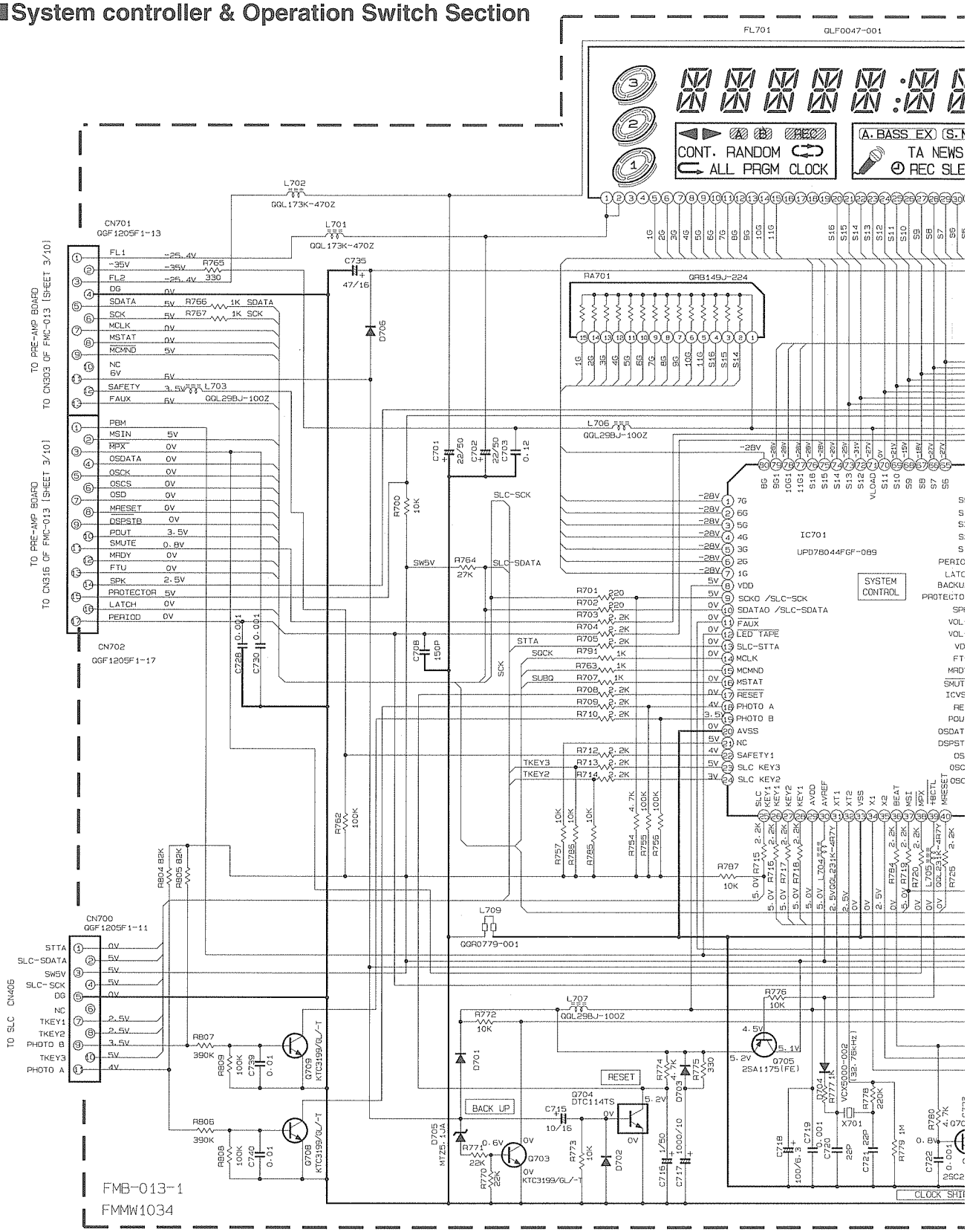
1. VOLTAGES ARE DC-MEASURED WITH A DIGITAL VOLT METER OR OSCILLOSCOPE WITHOUT INPUT SIGNAL.
   CONDITION ---- CD MODE
   VOLTAGE VALUE MARKED * IS IN TUNER POSITON

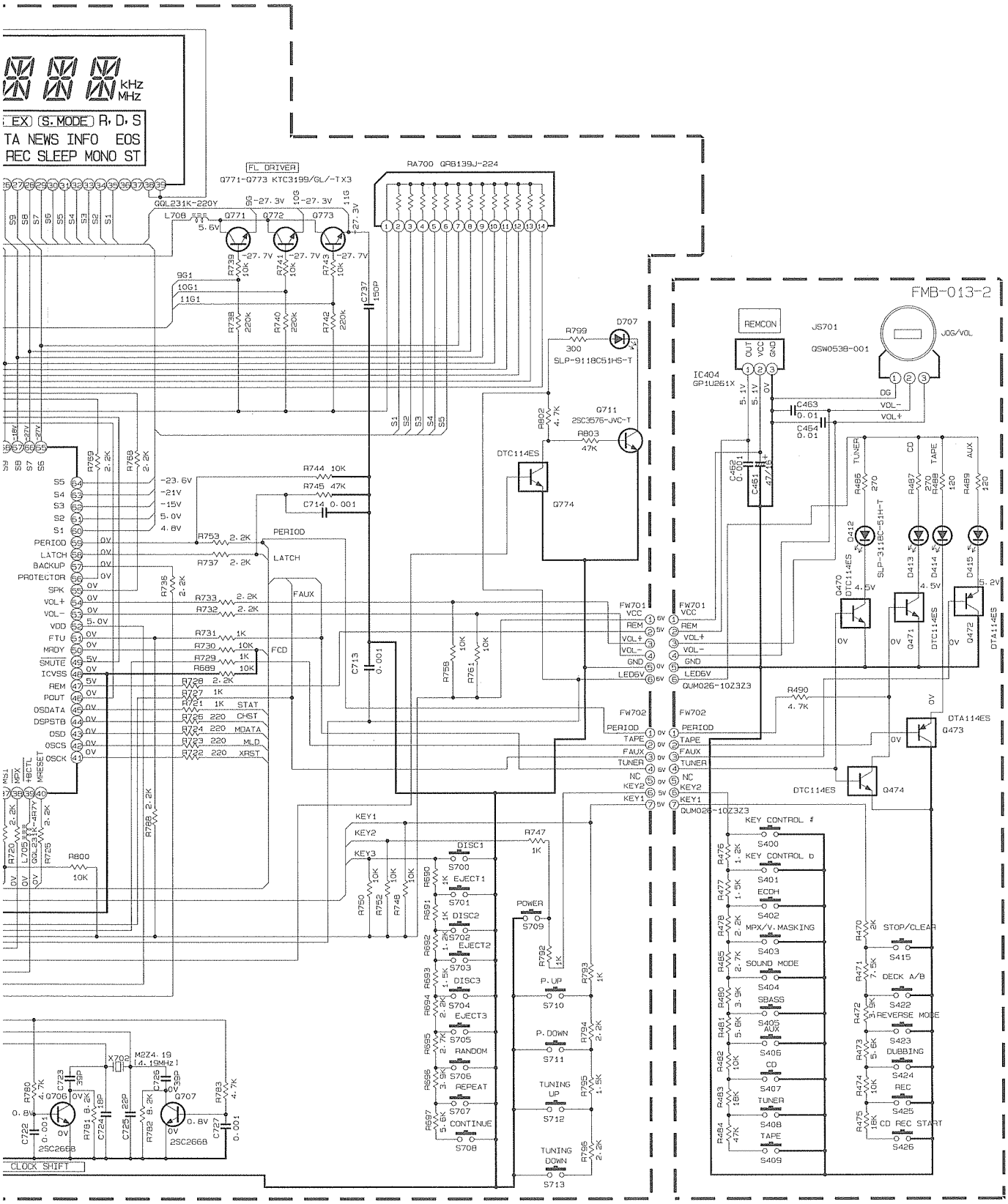
2. UNLESS OTHERWISE SPECIFIED, RESISTORS ARE 1/4W, 5% CARBON RESISTOR
   ALL RESISTANCE VALUES ARE IN OHM(Ω).
   ALL CAPACITORS ARE CERAMIC CAPACITOR OR MYLAR CAPACITOR.
   ALL CAPACITANCE VALUES ARE IN μF(P=pF).
   ALL INDUCTANCE VALUES ARE IN, H(m=mH).
   ALL E-CAPACITORS ARE SHOWN IN THE FORM OF CAPACITANCE (μF)/RATED VOLTAGE (V).
   ALL DIODES ARE 1SS133T-77 (NOT INDICATE DIODE)
   ALL NPN TRANSISTORS ARE 2SC3330(S,T) OR 2SC2785(E,F).

| SYMBOL \ VERSION | U,UB,UF,US | UT |
|---|---|---|
| C930 | 47/25 | 47/100 |
| FW501 | FW501 | CN313 |


FMC-013A
BASS BOOST AMP
BASS BOOST CTL
IC303 BA15218
IC901 BP5020
CD REG
TUNER REG
US5V REG
VIDEO OUT
CN308 GGB2526K1-11
FROM POWER AMP
FROM CN900 OF FMH-015-01 [SHEET 2/10]
CN307 GGB2526K1-08
FROM POWER AMP
FROM CN901 OF FMH-015-01 [SHEET 2/10]
CN309 GGD2501C1-03Z
FROM POWER BOARD
FROM FW906 OF FMH-015-01 [SHEET 2/10]
CN306 GGA2001C1-06
FROM VIDEO BOARD
FROM [SHEET9/10]
CN304 GGF1016C1-19
TO CD BOARD
TO CN651 OF CD BOARD [SHEET10/10]
CN316 GGF1201C3-17
FROM MICON SECTION
FROM CN702 OF FMB [SHEET 4/10]
TO TUNER SECTION
CN305 GGF1016C1-05
TO CD BOARD
TO CN652 OF CD BOARD [SHEET 10/10]
CD/MAIN SIGNAL
TAPE P.B. SIGNAL
TUNER SIGNAL

## System controller & Operation Switch Section





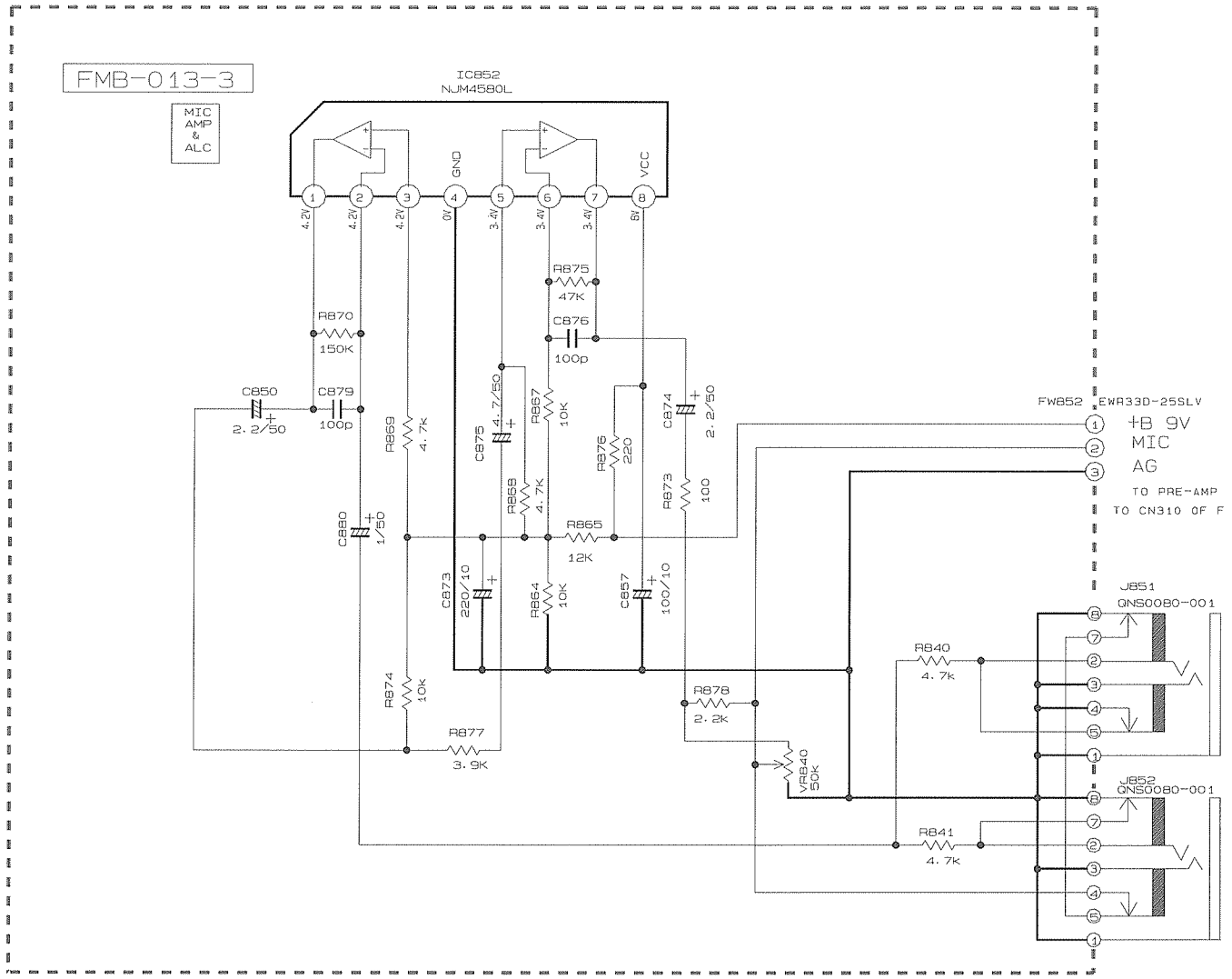

NOTES

1. VOLTAGES ARE DC-MEASURED WITH A DIGITAL VOLT METER OR OSCILLOSCOPE WITHOUT INPUT SIGNAL.
   CONDITION --- TAPE PB MODE
2. UNLESS OTHERWISE SPECIFIED
   RESISTORS ARE 1/4W ±5% CARBON RESISTOR
   ALL RESISTANCE VALUES ARE IN OHM(Ω).
   ALL CAPACITORS ARE CERAMIC CAPACITOR OR MYLAR CAPACITOR.
   ALL CAPACITANCE VALUES ARE IN #F(P=pF).
   ALL INDUCTANCE VALUES ARE IN #H(n=nH).
   ALL E-CAPACITORS ARE SHOWN IN THE FORM OF CAPACITANCE (#F)/RATED VOLTAGE (V).
   ALL DIODES ARE 1SS133

MODEL
MX-V508T / MX-V588T

F G H I J

## Mic & Headphone Section

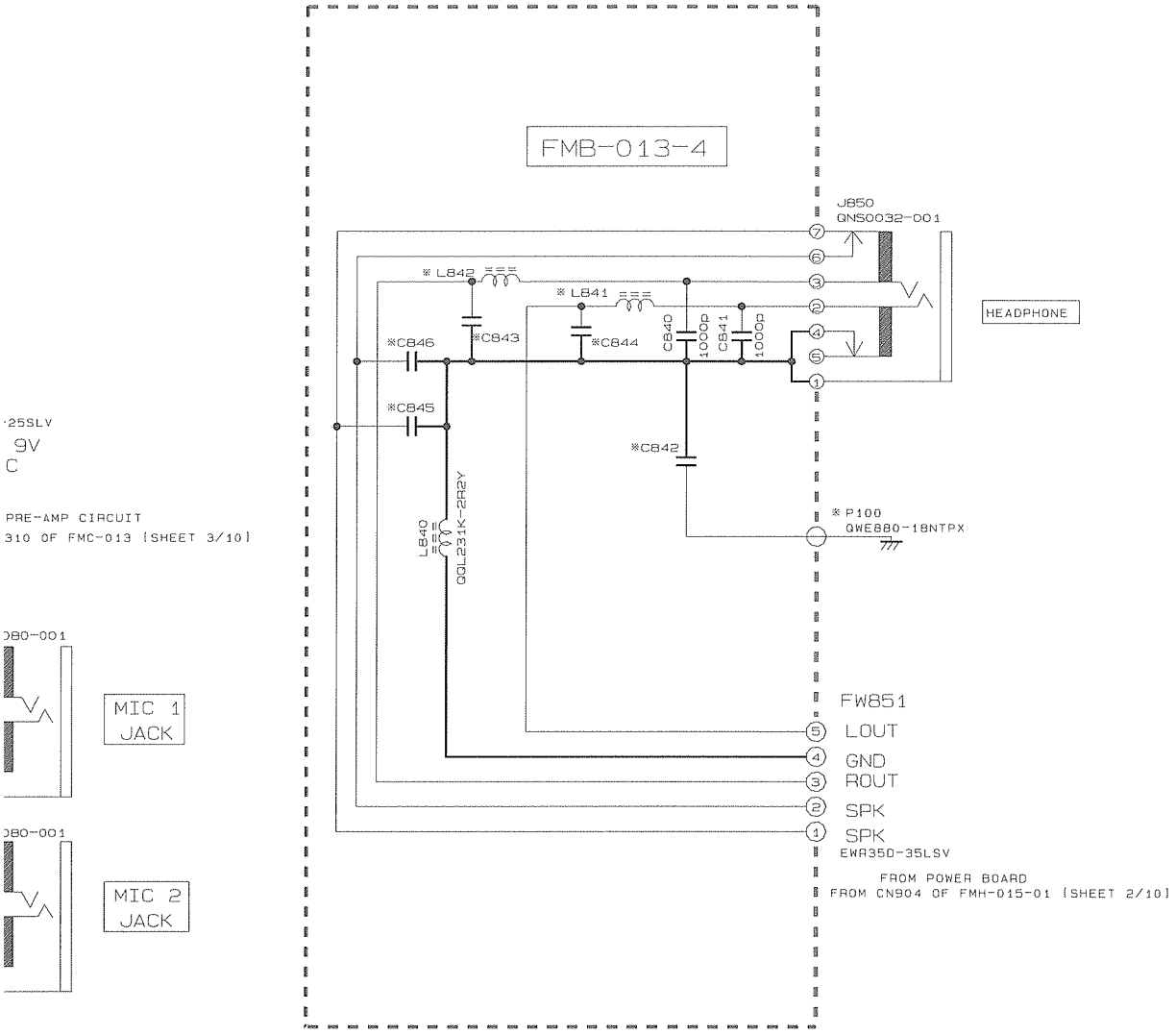



※ MARK

| VERSION | L841/L842 | C843/C844 C845/C846 | C842 |
|---|---|---|---|
| UT | 47u | 1000P | 1000P |
| OTHERS | B130/B131 | ——— | ——— |

NOTES

1. VOLTAGES ARE DC-ME OR OSCILLOSCOPE WI CONDITION --- TAPE ( )MEANS INVERT M
2. UNLESS OTHERWISE S 1/4W ± 5% CARBON R ALL RESISTANCE VAL ALL CAPACITORS ARE OR MYLAR CAPACITOR ALL CAPACITANCE VA ALL INDUCTANCE VAL ALL E.CAPACITORS A OF CAPACITANCE (μF ALL DIODES ARE 1SS



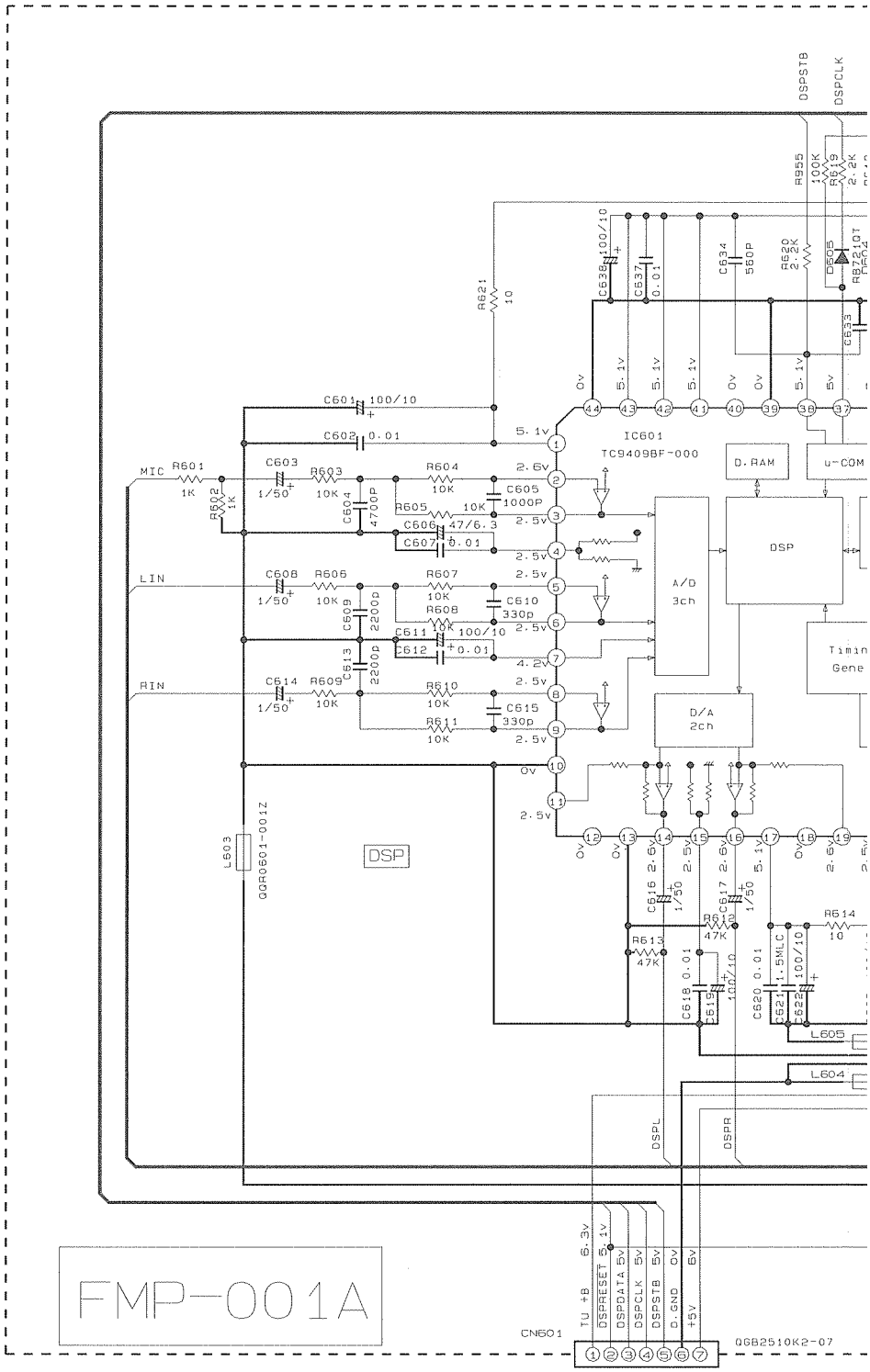

·C-MEASURED WITH A DIGITAL VOLT METER
·E WITHOUT INPUT SIGNAL.
TAPE STOP MODE
RT MODE.

SE SPECIFIED , RESISTORS ARE
·ON RESISTOR
VALUES ARE IN OHM(Ω).
ARE CERAMIC CAPACITOR
ITOR.
E VALUES ARE IN μF(P=pF).
VALUES ARE IN μH(m=mH).
·RS ARE SHOWN IN THE FORM
(μF)/RATED VOLTAGE (V).
1SS133T-77

MODEL
MX-V508T/MX-V588T

| F | G | H | I | J |
|---|---|---|---|---|

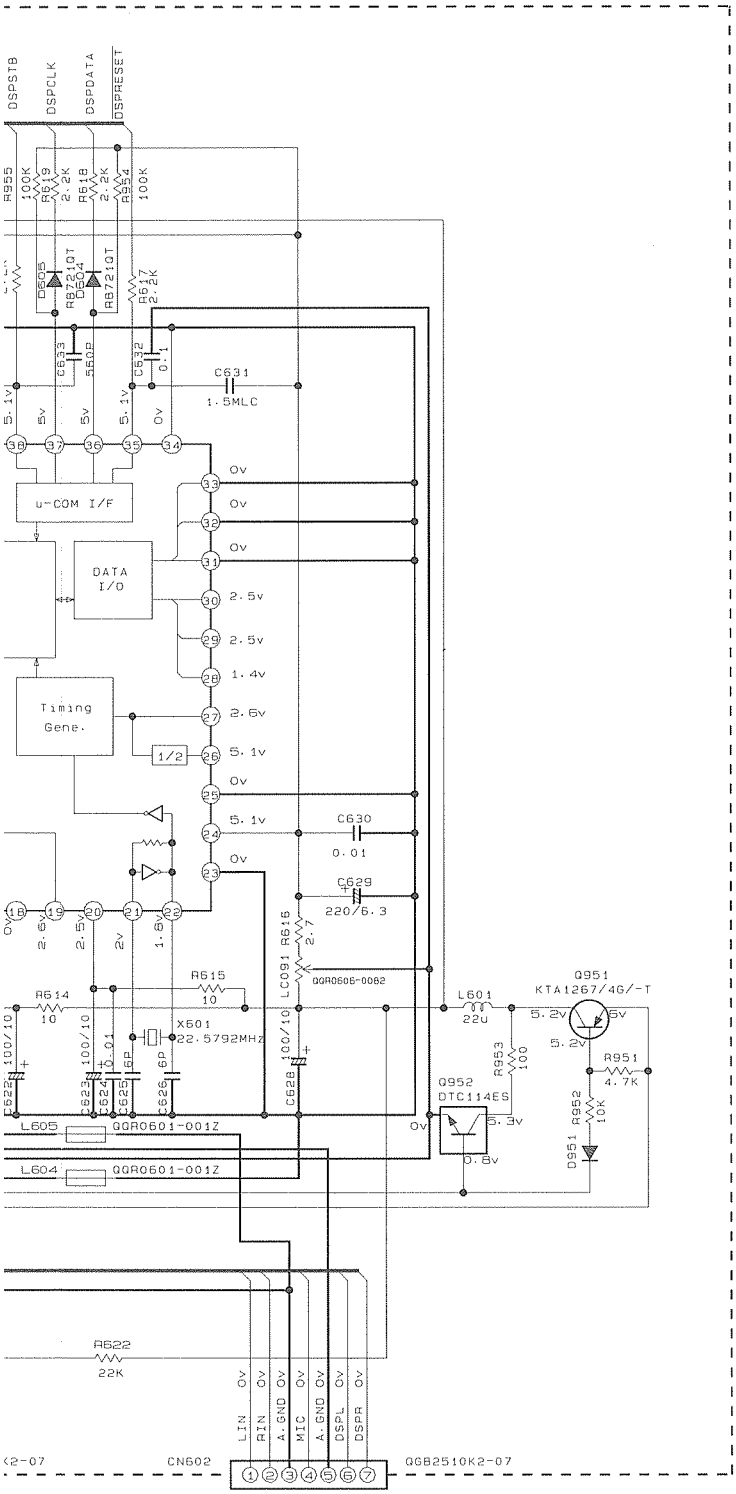
## DSP Section




NOTES

1. VOLTAGES ARE DC-MEASURED WITH A DIGITAL VOLT METER OR OSCILLOSCOPE WITHOUT INPUT SIGNAL.
   CONDITION --- TAPE STOP MODE
   ( )MEANS INVERT MODE.
2. UNLESS OTHERWISE SPECIFIED · RESISTORS ARE 1/4W ± 5% CARBON RESISTOR.
   ALL RESISTANCE VALUES ARE IN OHM(Ω).
   ALL CAPACITORS ARE CERAMIC CAPACITOR OR MYLAR CAPACITOR.
   ALL CAPACITANCE VALUES ARE IN μF(P=pF).
   ALL INDUCTANCE VALUES ARE IN μH(m=mH).
   ALL E.CAPACITORS ARE SHOWN IN THE FORM OF CAPACITANCE (μF)/RATED VOLTAGE (V).
   ALL DIODES ARE 1SS133T-77

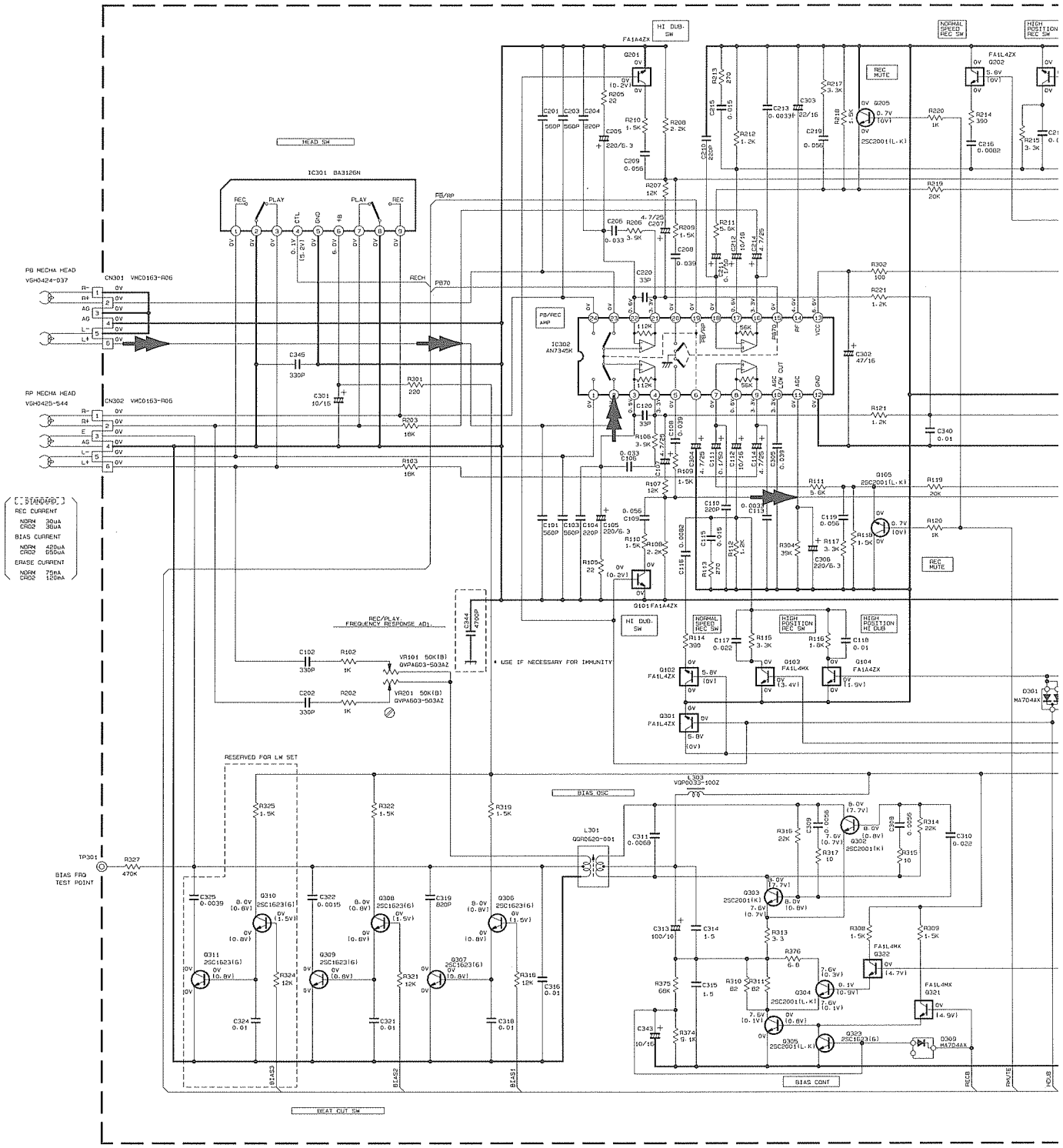
MODEL
MX-V508T.


DSPSTB
DSPCLK
DSPDATA
DSPRESET
R955 100K
R619 2.2K
R618 2.2K
R954 100K
D605 RB721QT
D604 RB721QT
R617 2.2K
C633 560P
C632 0.1
C631 1.5MLC
u-COM I/F
DATA I/O
Timing Gene.
1/2
C630 0.01
C629 220/6.3
R615 10
R614 10
X501 22.5792MHz
C622 100/10
C623 100/10
C624 0.01
C625 6P
C626 6P
C628 100/10
LC091 R616 2.7
QQR0606-0062
L601 22u
Q951 KTA1267/4G/-T
R953 100
R951 4.7K
Q952 DTC114ES
R952 10K
D951
L605 QQR0601-001Z
L604 QQR0601-001Z
R622 22K
LIN
RIN
A.GND
MIC
A.GND
DSPL
DSPR
CN602
QGB2510K2-07
FROM PRE-AMP BOARD
FROM CN312 OF FMC-013 [SHEET3/10]
3 [SHEET3/10]



| F | G | H | I | J |
|---|---|---|---|---|

# Head Amplifier & Mechanism Control Section




NOTES

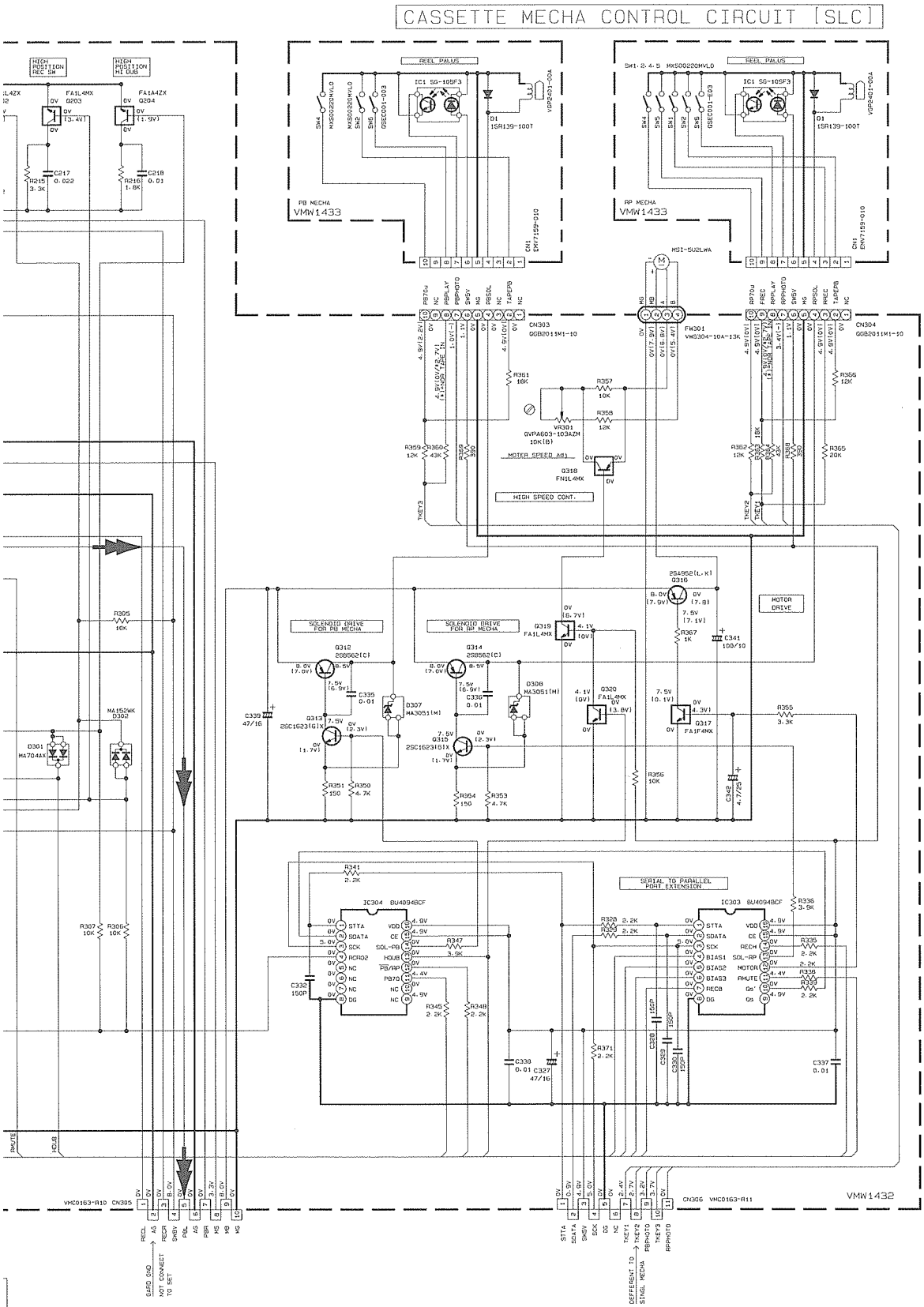
1. VOLTAGES ARE DC-MEASURED WITH A DIGITAL VOLT METER OR OSCILLOSCOPE WITHOUT INPUT SIGNAL. ( ) IS INVERT MODE
2. UNLESS OTHERWISE SPECIFIED
   ALL RESISTANCE VALUES ARE IN OHM(Ω).
   ALL CAPACITORS ARE CERAMIC CAPACITOR
   ALL CAPACITANCE VALUES ARE IN μF(P=pF).
   ALL INDUCTANCE VALUES ARE IN #H(m=mH).
   ALL E.CAPACITORS ARE SHOWN IN THE FORM OF CAPACITANCE (μF)/RATED VOLTAGE (V).
   PP PLYPROPYLENE CAPACITOR

TABLE 1. DIGITAL TR LIST

| PART NO | CONSTRUCTION | REF. NO | | | |
|---|---|---|---|---|---|
| FN1L4M | 47K 47K | Q318 | FA1F4M | 22K 22K | Q317 |
| FA1A4Z | 10K | Q101/Q201 Q104/Q204 | FA1L4M | 47K 47K | Q103/Q203 Q319 Q320/Q321/Q322 |
| FA1L4Z | 47K | Q102/Q202 Q301 | | | |

A B C D E

# CASSETTE MECHA CONTROL CIRCUIT [SLC]

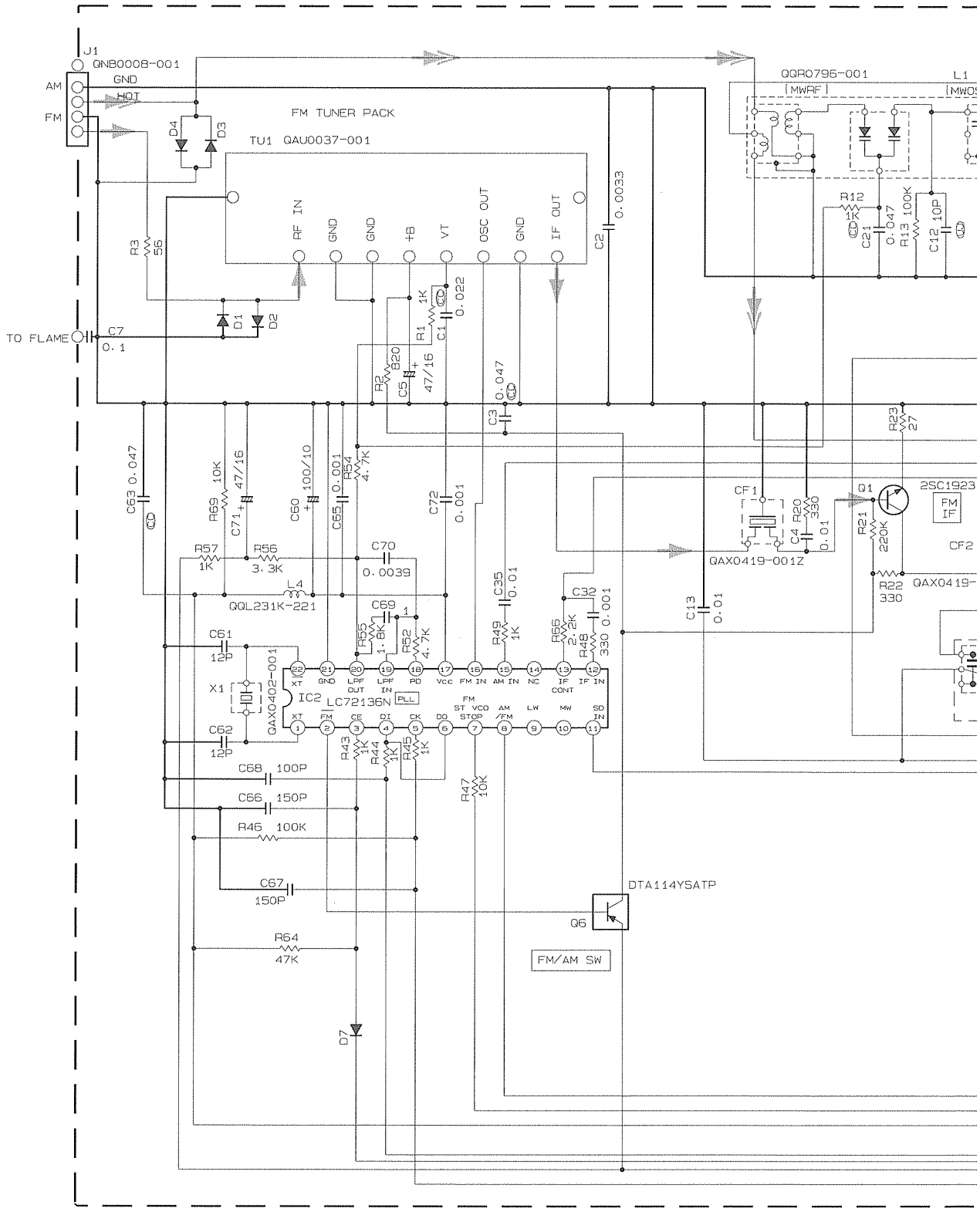



MODEL

MX-V508T/MX-V588T

| F | G | H | I | J |
|---|---|---|---|---|

## ■TUNER Section

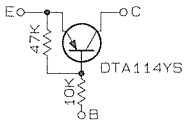



| CONDITION PIN NO. | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IC1 | FM NO SIGNAL | 2.0 | 0.5 | 0 | 2.0 | 6.2 | 6.2 | 0 | 0 | 0.2 | 6.2 | 5.8 | 1.0 | 1.0 | 5.5 | 4.8 | 4.8 | 1.4 | 0 | 1.3 | 1.1 | 2.0 | 2.0 | 6.2 | 2.0 |
| | FM 60dB STEREO | 2.0 | 0.5 | 0 | 2.0 | 6.2 | 6.2 | 1.1 | 0 | 0.2 | 0 | 0 | 1.0 | 1.0 | 5.5 | 4.8 | 4.8 | 1.4 | 0 | 1.4 | 1.1 | 2.0 | 2.0 | 6.2 | 2.0 |
| | AM NO SIGNAL | 2.0 | 0.5 | 0 | 2.0 | 6.0 | 6.2 | 0 | 0 | 0.2 | 6.2 | 5.8 | 1.0 | 1.0 | 5.7 | 2.9 | 0 | 1.4 | 1.4 | 1.5 | 1.5 | 2.0 | 2.0 | 6.2 | 2.0 |
| IC2 | FM NO SIGNAL | 3.1 | 0 | 0.9 | 5.2 | 5.2 | 5.2 | 4.8 | 4.8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 3.1 | 6.2 | 1.0 | 1.0 | 2.0 | 0 | 3.0 | | |

| Tr NO. |
|---|
| PIN NO. |
| FM 87.5MHz NO S |
| AM 531KHZ NO S |

NOTES

1. VOLTAGES ARE DC-MEASURED WITH A DIGITAL VOLT METER.
2. ALL RESISTORS ARE 1/4W 5% CARBON RESISTOR.
3. ALL RESISTANCE VALUES ARE IN OHM(Ω).
4. ALL CAPASITANCE VALUES ARE IN μF(P=pF).
5. ALL E.CAPASITORS ARE SHOWN IN THE FORM OF CAPASITANCE (μF)/RATED VOLTAGE (V).
6. SI.DIODES( ) ARE ALL 1SS133T
8. INSIDE OF DIGITAL TRANSISTORS ARE SHOWN AS FOLLOWS.







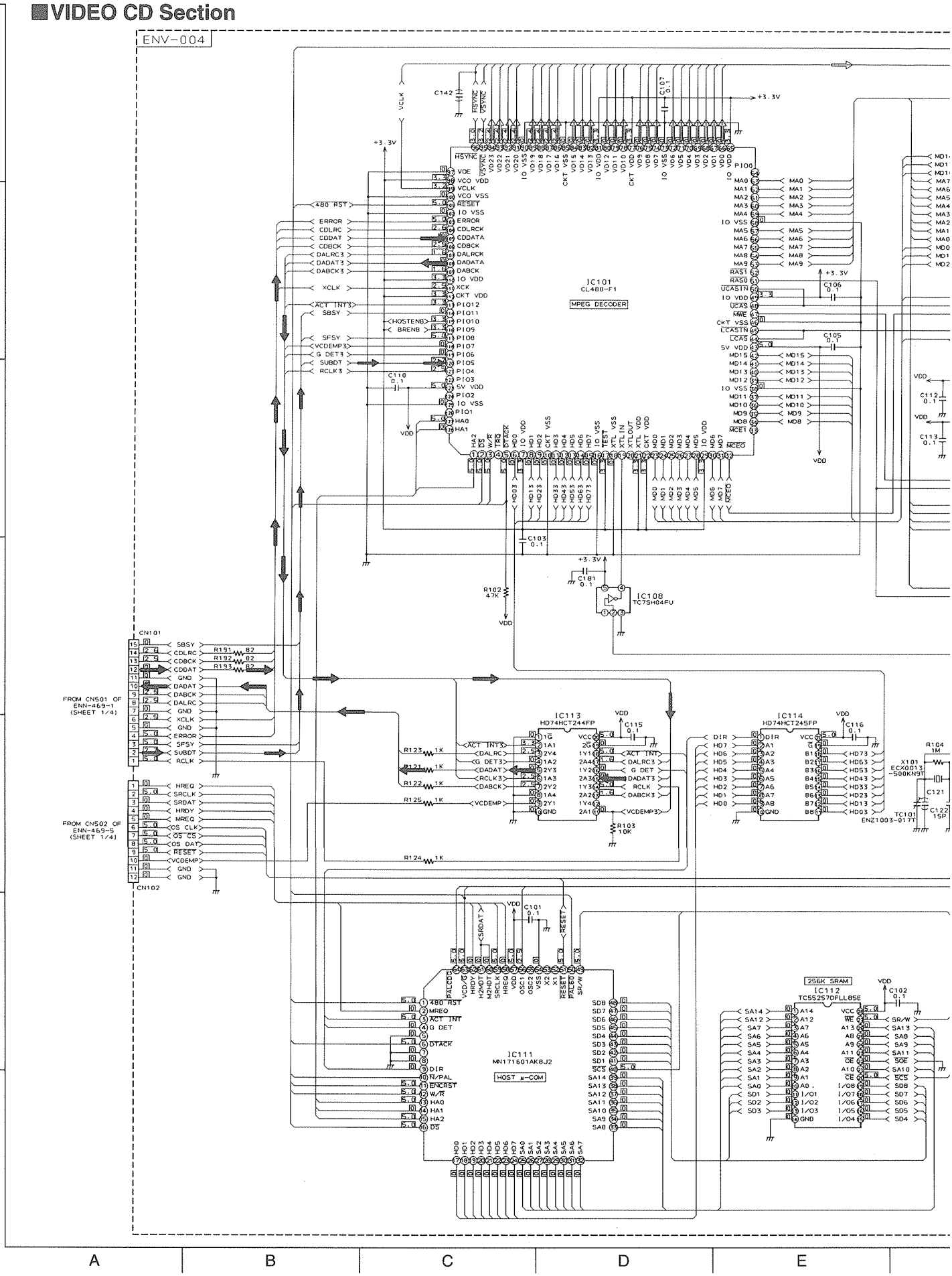
| r NO. | Q1 | | | Q6 | | |
|---|---|---|---|---|---|---|
| IN NO. | E | C | B | E | C | B |
| MHz NO SIGNAL | 0 | 7.8 | 0.8 | 9.1 | 9.0 | 0 |
| KHZ NO SIGNAL | 0 | 0.4 | 0.4 | 9.1 | 0.4 | 9.0 |

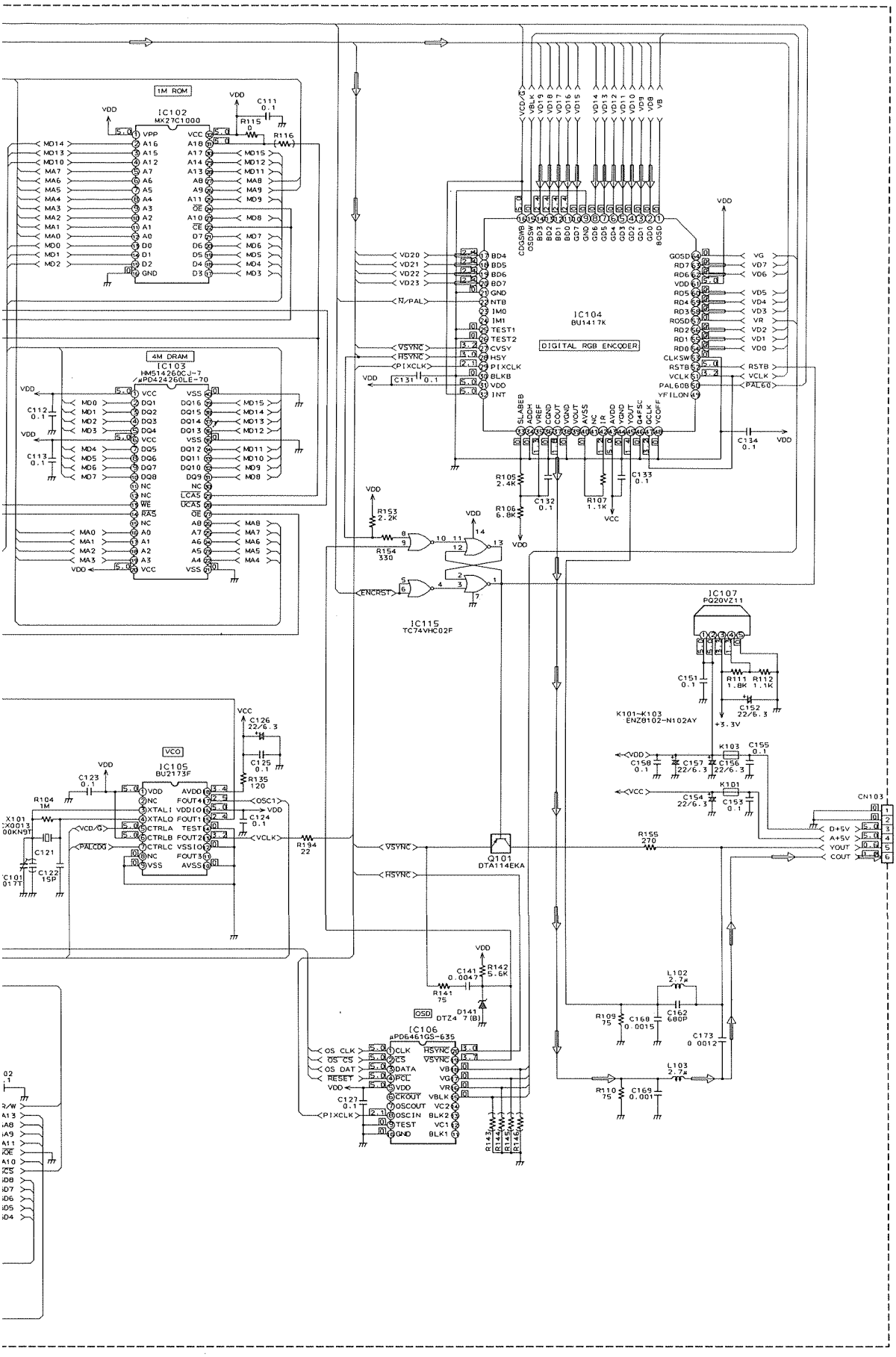
MX-V588T
MX-V508T

FM/TUNER MAIN SIGNAL
AM SIGNAL

F G H I J

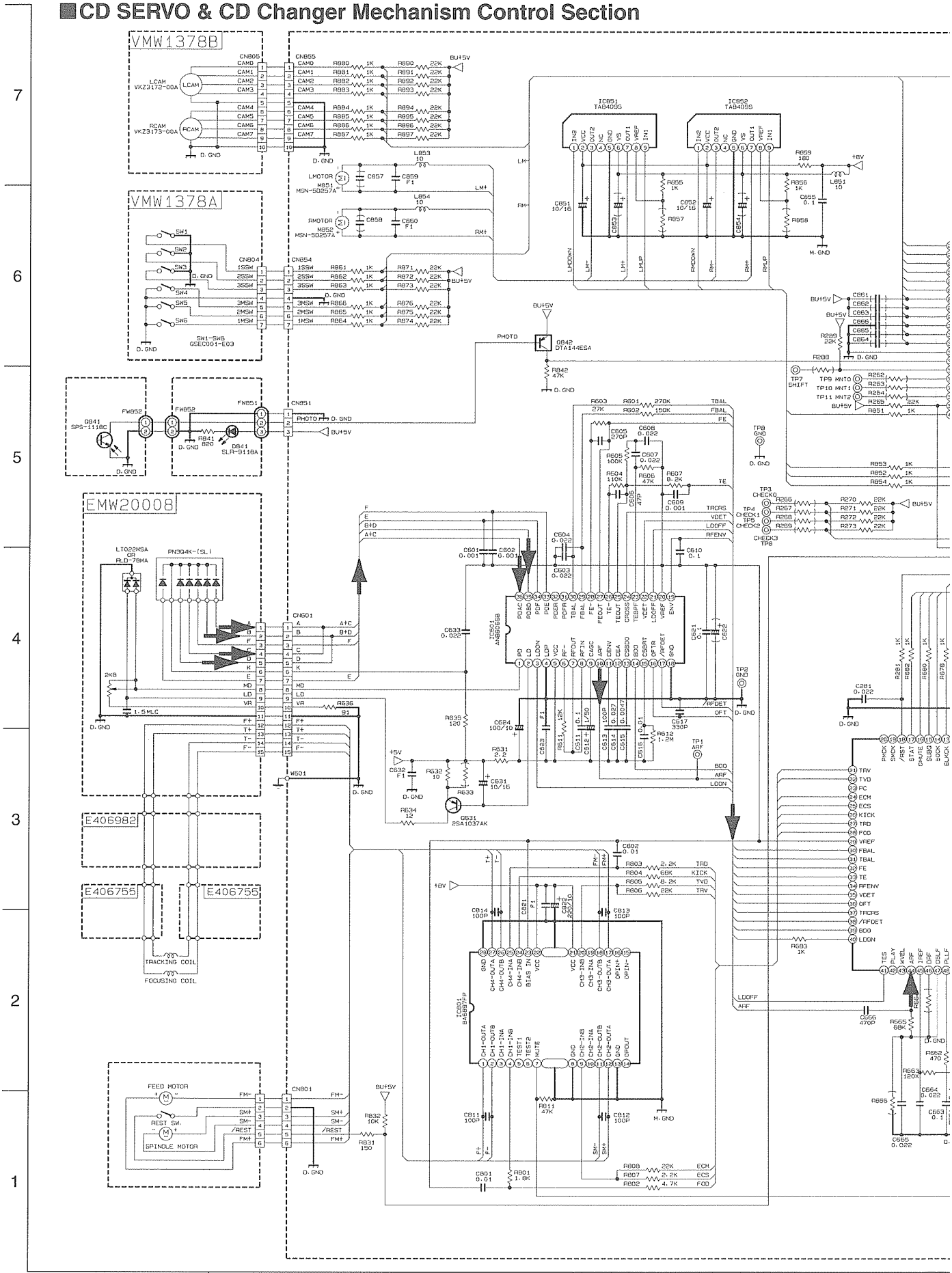
# ■VIDEO CD Section

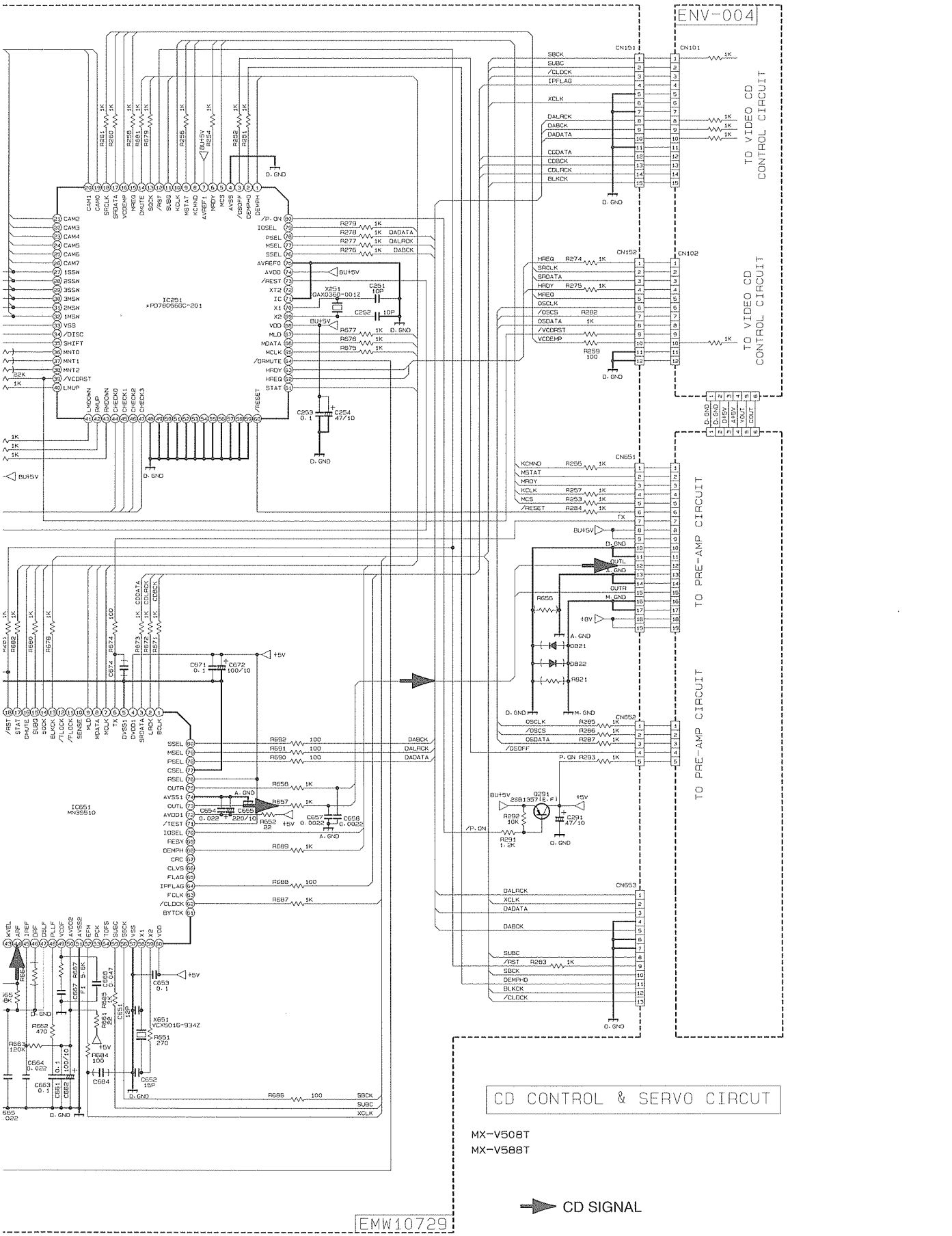



1M ROM
IC102
MX27C1000
4M DRAM
IC103
HM514260CJ-7
μPD424260LE-70
IC104
BU1417K
DIGITAL RGB ENCODER
IC115
TC74VHC02F
IC107
PG20VZ11
IC105
BU2173F
VCO
IC106
μPD6461GS-635
OSD
Q101
DTA114EKA
K101~K103
ENZ8102-N102AY
+3.3V
CN103
FROM CN503 OF
ENN-469-1
(SHEET 1/4)
VDD
VCC
ENCRST
HSYNC
VSYNC
PIXCLK
VCLK
PAL60
YFILON

F G H I J

## CD SERVO & CD Changer Mechanism Control Section




ENV-004
TO VIDEO CD CONTROL CIRCUIT
TO PRE-AMP CIRCUIT
CD CONTROL & SERVO CIRCUT
MX-V508T
MX-V588T
CD SIGNAL
EMW10729
IC251 μPD78065GC-201
IC651 MN35510
X651 VCX5016-934Z
X251 GAX0360-001Z
Q291 2SB1357(E,F)
CN151
CN101
CN152
CN102
CN651
CN652
CN653
D. GND
A. GND
M. GND
BU+5V
+5V
+8V

F | G | H | I | J